The Circuit for Z-80s

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The microprocessor integrated circuit is the real engine for your system. Now you can replace that old engine with a real power house, the new Z-80 (the Z-80 was described in Burt Hashizume's Microprocessor Update on page 34 of August 1976 BYTE). After initially reading about this integrated circuit in early '76, I just had to get one to see how many of the blurbs were true (I give sales advertisements a 1% credibility on the first pass).

Aside from a few typos, promised support chips that didn't show, and several mistakes in the software documentation, it was fabulous. The software flexibility added by this chip was a great addition to the 8080/6502/6800 Digital Group stable. The relative branch was very helpful for machine language programming, and the ability to test, set, and clear individual bits in a byte has opened a new world of control applications. I saw a 20% savings in memory requirements even though I was still new to much of the Z-80's special software.

The Z-80's hardware made good sense too. Getting rid of the 18 MHz crystal requirement of the 8224/8080 system and using a 2.5 MHz crystal with a simple single phase TTL clock made me happy. The interrupt and DMA system has some neat features. Sure gonna be hard to justify using the old 8080/6502 or 6800 CPU boards any more, thought I, as I set out to design the circuit for Z-80s.

The circuit for Z-80s presented in this article is the actual wiring used in the Digital Group's Z-80 processor card. Not too unbelievably, we would just love to sell you the whole system. The circuit is being published in complete detail for your information, whether you choose to purchase it as part of your system, or use it as a starting point for your own custom design. The systems approach to microprocessors which I described in the June 1976 BYTE [*page 32*] is reflected in the design of this central processor circuit.

This Z-80 circuit is shown in figures 1 and 2. In figure 1 you'll find the central processor integrated circuit (IC43, a Z-80 made by Zilog or second source Mostek), and miscellaneous drivers, decoders and gates. In figure 2 you'll find the wiring of 2 K bytes of programmable memory along with a 256 byte 1702A erasable read only memory which can be used to store the bootstrap programs for your system.

Full direct memory access (DMA) is used in this design. What's DMA to you? Well for one thing, DMA permits hand loading of the memory from a front panel which is completely independent of a particular processor. It permits future processor upgrading by replacing a single board. High speed data devices, such as some tape, disk, and video systems which may operate too fast for most processors, can directly load memory using DMA. Finally, for the truly gigantic among you, multiple processors can share common memory with the addition of control logic.

Buffering is included on this processor board design to permit driving a full memory system (64 K bytes) and up to 256 IO ports. Miscellaneous logical functions such as power on reset and single stepping are provided.

The EROM bootstrap provides a convenient way to initialize the system at power on, by using a low cost cassette [*page 46, July 1976 BYTE*]. We use an EROM in the design in order to allow customized initialization by sophisticated users able to program their own EROMs. Circuitry to inhibit EROM selection is included in order to permit full use of "0 page" programmable memory for user software.

Two K bytes of programmable random access memory give sufficient storage for a small operating system. The Digital Group Z-80 system includes a cassette which loads this area of programmable memory with a system monitor which permits reading and

When inserting large integrated circuits into sockets, avoid uneven stresses. In extreme cases of uneven insertion pressure, it is possible to crack the case of a 24 or 40 pin integrated circuit, rendering it useless.

writing other cassettes, keyboard entry of data and programs, and TV display of memory data, all 14 registers, indices, and flags (in octal or hexadecimal).

The system used to interface this processor to memory and IO exemplifies the "processor independence" ideal mentioned in my article in the June BYTE. Two sets of 16 address lines are brought out from each Digital Group processor card. The 16 lines labeled "memory address" in figure 1 lead to the memory boards; the 16 lines labeled "port address" in figure 2 go to the IO port selecting card(s). Similarly, memory data to and from the processor is separated, as is the peripheral IO data to and from the processor.

The Z-80 DMA read, write and IO lines are brought to decoding logic to derive your universal control lines, ie: memory read ($\overline{MRD}$), memory write ($\overline{MWR}$), IO read ($\overline{IORD}$), and IO write ($\overline{IOWR}$).

The major objective of processor independency is supported by providing this common set of 32 address lines, 32 data lines, and 4 control lines for each processor. It is the responsibility of the processor board to provide the logical derivation of these 68 lines. The complete list of backplane connections for the system includes all 68 logic lines and is summarized in table 1. The rest of the system is interfaced to this common 68 line system. Processor interchange is thus particularly simple: It is achieved by plugging in a different processor card.

Z-80 Processor Circuit

The logic of this Digital Group Z-80 processor circuit may be logically divided into six interrelated sections. They are the processor itself and immediate "housekeeping" logic, run control, DMA, interrupt, buffering, and memory. The processor and immediate housekeeping consists of the Z-80, a 7400 single phase crystal controlled clock generator, and decoders for read, write, memory and IO operations. These are all found in figure 1.

A power on reset function is provided by IC38d, one section of a 4010 CMOS buffer. An external switch is attached to the backplane assembly for a remote "reset and go" operation after power has been applied.

A 7442, IC48, decodes IO states of the processor: memory reading, memory writing, input port reading, and output port writing. Each of these signals occurs at the proper time as determined by the processor.

Run control logic permits single stepping through a program if a front panel readout is provided for viewing the resulting instruction sequencing. In addition, wait states for slow external memory and the EROM access delay are provided. The wait line input of the Z-80 is utilized to control execution. A feature of this Z-80 circuit is the ability to jumper select either "single step" or "step on instruction." The jumpering for "single steps" permits stepping within an instruction cycle in the same manner as the 8080. "Step on instruction" will display only the first byte of each single or multibyte instruction. Normal processor running mode is unaffected by which stepping mode is selected.

Two sections of a 7402, IC28a and IC28b, are used as a run latch. When the step switch is activated, the run latch is reset, and the one shot (74123, IC37b) fires a 50 ms pulse to debounce the switch. The resultant pulse is held in a 7474 latch section, IC29a, for a very short time until synchronized by the Z-80 and acknowledged through the second oneshot section of IC37. The 7402 NOR gate IC28c passes either the continuous run or the step pulse depending on the mode selected. IC28d will then drop the ready line if either no run command exists (continous or step), or the "wait" command line goes high. If no "single step" operation is to be used, pin 43 of the backplane is tied to +5 V externally.

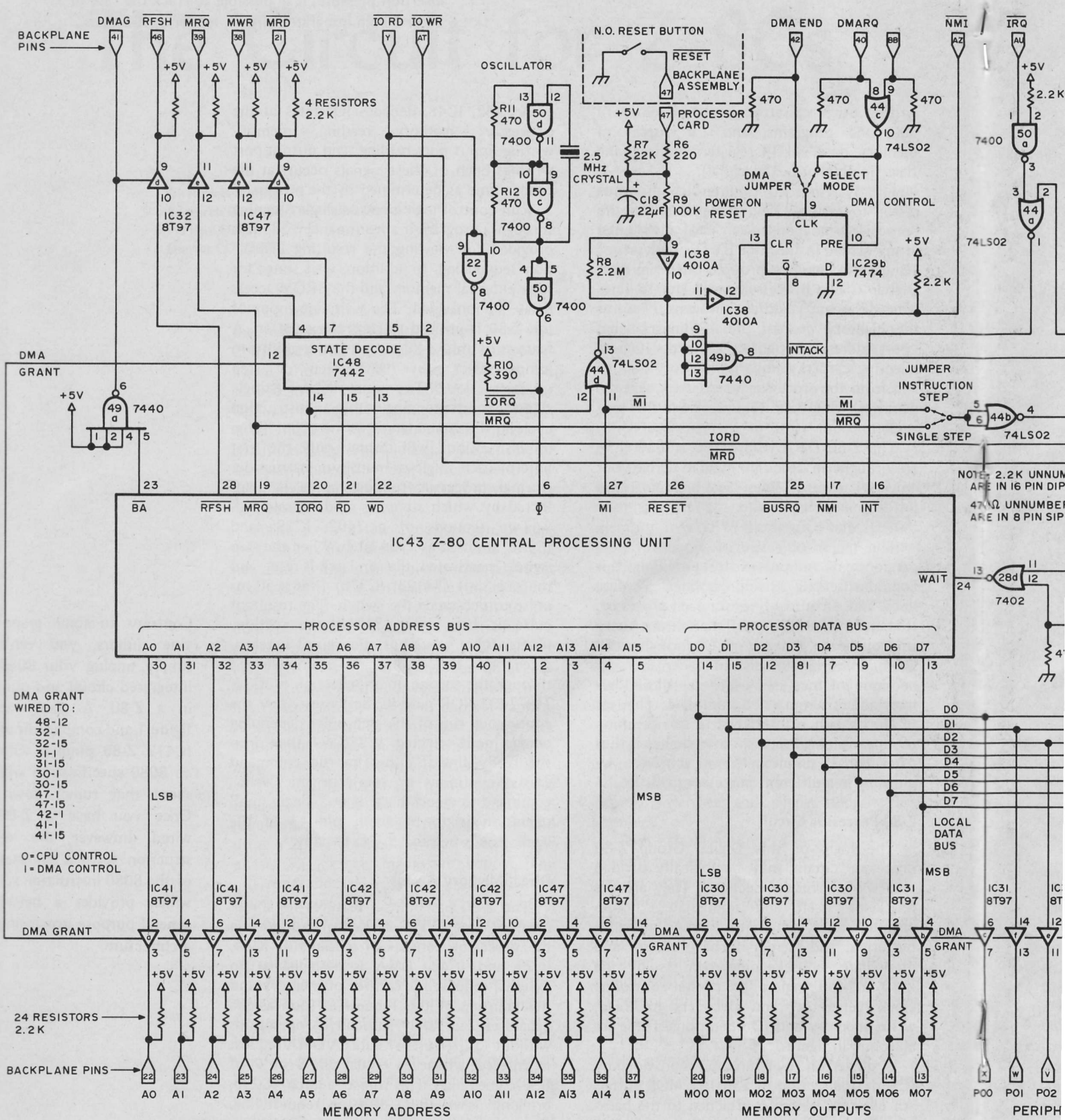
Direct Memory Access

The Z-80 has built-in features for direct memory access. The DMA logic supporting the processor consists of sections of IC44, IC29 and IC49. DMA is designed as an external request for control of memory and the granting of this request as soon as the processor can safely suspend its operations without losing current data. A DMA request is entered whenever either pin 8 or 9 of IC44c goes high. This will set a latch, IC29b, bringing down the Z-80's bus request line.

Text continued on page 68

Contrary to some grapevine rumors, you can't simply unplug your 8080 integrated circuit and plug in a Z-80. A glance at figure 1 and comparison of IC43's Z-80 pinouts with an 8080 specification will shoot that rumor down. Once you have a Z-80 wired, however, the instruction set is a superset of the 8080 instruction set which provides a better general purpose processing architecture.

Figure 1: The central processor of the Z-80 circuit. See also figure 2 for the balance of the logic found in the Digital Group Z-80 central processor card. This figure contains the processor integrated circuit, IC43, and ancilliary logic of the system clock, buffers, run control, interrupts and direct memory access control. A summary of back plane connections is found in table 1 accompanying



this article. The complete list of power connections for both figures 1 and 2 is found in table 2. This schematic was redrawn to fit the constraints of the magazine page. A complete schematic in its original form, drawn on one page, is included with the documentation of the Digital Group Z-80 central processor kit.

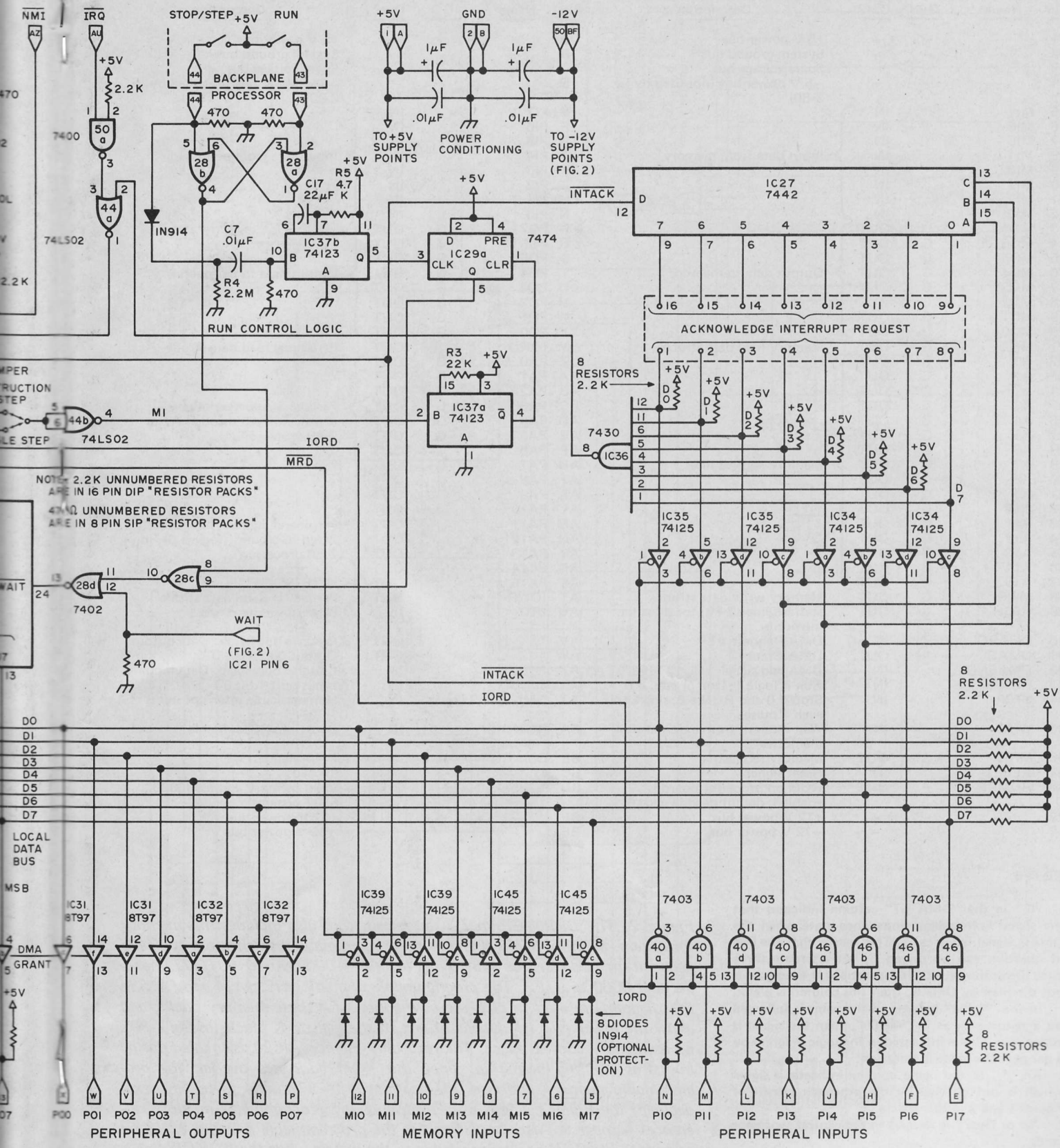


Table 1: A Generalized Processor Independent Bus Structure. This table lists connector pin identification, signal name, DMA access properties, primary signal direction relative to the processor card, and description. This is the bus definition used in the Digital Group systems.

Pin	Name	DMA G?	In or Out?	Description	Pin	Name	DMA G?	In or Out?	Description
1	–	–	–	+5 V power bus	A	–	–	–	+5 V power bus
2	–	–	–	System ground bus	B	–	–	–	System ground bus
3	–	–	–	Spare voltage bus	C	–	–	–	Spare voltage bus
4	–	–	–	–5 V power bus (not used by Z-80)	D	–	–	–	–5 V power bus (not used by Z-80)
5	MI7		IN		E	PI7		IN	
6	MI6		IN		F	PI6		IN	
7	MI5		IN		H	PI5		IN	
8	MI4		IN	Input data from memory	J	PI4		IN	Input data from peripherals
9	MI3		IN		K	PI3		IN	
10	MI2		IN		L	PI2		IN	
11	MI1		IN		M	PI1		IN	
12	MI0		IN		N	PI0		IN	
13	MO7	G	OUT		P	PO7	G	OUT	
14	MO6	G	OUT		R	PO6	G	OUT	
15	MO5	G	OUT		S	PO5	G	OUT	
16	MO4	G	OUT	Output data to memory	T	PO4	G	OUT	Output data to peripherals
17	MO3	G	OUT		U	PO3	G	OUT	
18	MO2	G	OUT		V	PO2	G	OUT	
19	MO1	G	OUT		W	PO1	G	OUT	
20	MO0	G	OUT		X	PO0	G	OUT	
21	MRD-	G	OUT	Memory read data strobe	Y	IORD-		OUT	Peripheral read data strobe
22	A0	G	OUT		Z	PA0	G	OUT	
23	A1	G	OUT		AA	PA1	G	OUT	
24	A2	G	OUT		AB	PA2	G	OUT	
25	A3	G	OUT		AC	PA3	G	OUT	Peripheral address, low order, identical to A0 through A7 in Z-80 processor.
26	A4	G	OUT		AD	PA4	G	OUT	
27	A5	G	OUT		AE	PA5	G	OUT	
28	A6	G	OUT		AF	PA6	G	OUT	
29	A7	G	OUT	Memory address lines	AH	PA7	G	OUT	
30	A8	G	OUT		AJ	PA8		OUT	
31	A9	G	OUT		AK	PA9		OUT	
32	A10	G	OUT		AL	PA10		OUT	
33	A11	G	OUT		AM	PA11		OUT	Peripheral address, high order, wired to ground **(logical 0)** in Z-80 processor.
34	A12	G	OUT		AN	PA12		OUT	
35	A13	G	OUT		AP	PA13		OUT	
36	A14	G	OUT		AR	PA14		OUT	
37	A15	G	OUT		AS	PA15		OUT	
38	MWR-	G	OUT	Memory write data strobe	AT	IOWR-		OUT	Peripheral write data strobe
39	RFSH-	G	OUT	Refresh line (Z-80) for dynamic memories	AU	IRQ-		IN	Interrupt request line
40	DMARQ		IN	DMA Request #1	AV	*		OUT	Cassette bootstrap: Data output
41	DMAG		OUT	DMA Grant	AW	*		OUT	Output port 1 bit 0
42	DMAEND		IN	DMA end signal	AX	*		IN	Cassette bootstrap: Data input
43	RUN		IN	Run if logic 1, stop or step if 0	AY	*		IN	Input port 1 bit 0
44	STEP		IN	Stop if 0 and RUN = 0; single step each 1 pulse.	AZ	NMI-		IN	Non maskable interrupt input
45	WRQ-		IN	Wait request, from external slow memories	BA	ROMDIS		IN	Bootstrap ROM disable
46	MRQ-	G	OUT	Memory request	BB	DMARQ		IN	DMA Request #2
47	RESET-		IN	Reset signal	BC	–	–	–	unused
48	ROMCE-		OUT	ROM on processor board is enabled; do not decode page 0.	BD	*		OUT	Valid memory address (6800, 6502 systems)
49	–	–	–	+12 V power bus	BE	–	–	–	+12 V power bus
50	–	–	–	–12 V power bus	BF	–	–	–	–12 V power bus

NOTES:

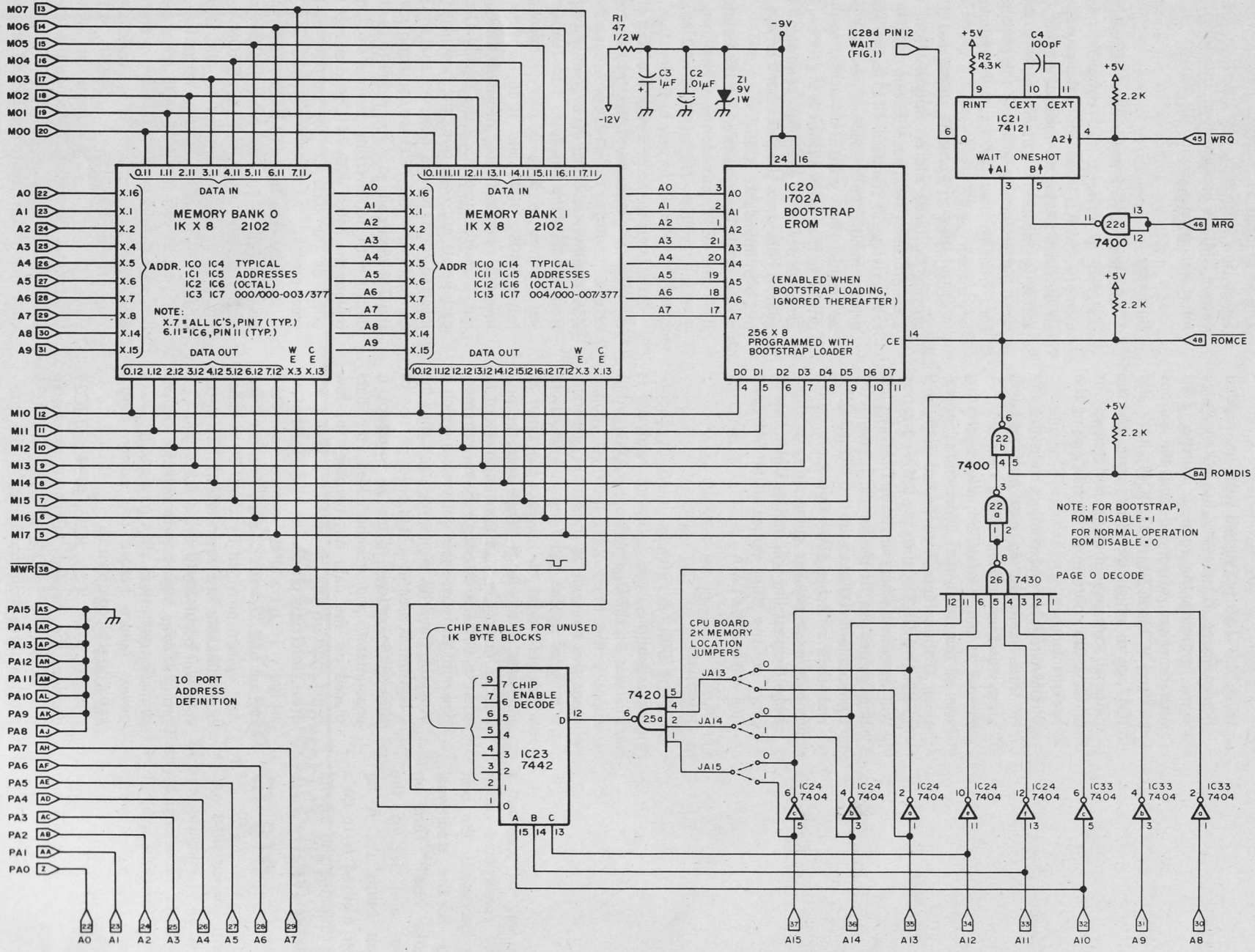
"G" in the "DMA G?" column indicates that the signal is in a high impedance state when the DMAG signal is logical 1. This means that the line in question can be driven by an alternate three state driver during a DMA operation. If the signal is not disabled by DMAG, then this column is blank.

In the "Name" column, if the name is followed by a minus sign as in "MRD-", then the signal is active low. This is indicated in the logic diagram by a bar over the name in question.

An "*" in the name column indicates a signal which is not defined by the processor circuit of figures 1 and 2 in this article.

"In or Out?" is relative to the central processor card.

Figure 2: The Digital Group Z-80 processor card also includes this memory subsystem. Memory banks 0 and 1 are programmable user memory typically decoded to addresses at split octal locations 000/000 to 007/377, hexadecimal 0000 to 07FF. The programmable jumpers JA13, JA14 and JA15 in this diagram are used to pick the base address for these memory banks, and allow the lower two 1 K blocks of any of the eight 8 K blocks in the Z-80's 64 K memory address space. The read only memory, IC20, is enabled during bootstrap. During bootstrap, since the ROM addresses overlap the programmable memory addresses at locations 0 to 377 octal (0 to FF hexadecimal) the ROMCE line is used to disable any programmable memory references to page 0. After bootstrapping the programmable memory exclusive of page 0, the ROM becomes invisible to the system when the ROMDIS line is in a high state. (This line should be controlled by a manual switch.)


MEMORY BANK 0
IK X 8 2102
MEMORY BANK 1
IK X 8 2102
IC20
1702A
BOOTSTRAP
EROM
(ENABLED WHEN
BOOTSTRAP LOADING,
IGNORED THEREAFTER)
256 X 8
PROGRAMMED WITH
BOOTSTRAP LOADER
IC21
74121
IC23
7442
CHIP
ENABLE
DECODE
7420
7430
7400
IC24
7404
IC33
7404
-9V
-12V
+5V
2.2K
R1
47
1/2W
R2
4.3K
C3
1μF
C2
.01μF
C4
100pF
Z1
9V
1W
IC28d PIN12
WAIT
(FIG.1)
WRQ
MRQ
ROMCE
ROMDIS
PAGE 0 DECODE
NOTE: FOR BOOTSTRAP,
ROM DISABLE = 1
FOR NORMAL OPERATION
ROM DISABLE = 0
CHIP ENABLES FOR UNUSED
IK BYTE BLOCKS
CPU BOARD
2K MEMORY
LOCATION
JUMPERS
JA13
JA14
JA15
IO PORT
ADDRESS
DEFINITION
MWR

Text continued from page 63

When the Z-80 is finished with any needed housekeeping, it issues the bus acknowledge signal, granting the request. Further Z-80 operations are suspended and the various buffers, IC31, IC32, IC33, IC41, IC42 and IC47, go to a high impedance state, and the external circuitry making the request is allowed full control over memory using the backplane bus.

DMA request and grant is ended by any of three methods. A reset operation will always end any current DMA operation. A jumper at pin 9 of IC29b allows selecting one of the other two DMA ending operations. If the jumper is connected from pin 9 to pin 10 of IC29b, then the DMA operation will be ended whenever both DMA request lines return low. If the jumper is connected from pin 9 of IC29b to the line labeled DMA end, then a latched DMA operation results. One or more positive going pulses at either DMA Request line will initiate DMA. One or more positive going pulses at the DMA end line will end the DMA.

Interrupts

The Z-80 has extended interrupt processing capabilities, and sufficient hardware is included on the Digital Group Z-80 board to support the three Z-80 interrupt modes. Mode 0 is the same as the 8080A, generally considered as the eight restart instructions which are placed on the data bus upon an interrupt acknowledge signal from the processor. Mode 1 is an automatic interrupt to address 000070. Mode 2 is an extremely powerful vectored interrupt system which is new with the Z-80. A new register, called the I register, is used as a high order portion of the vector address. When an interrupt is encountered and acknowledged, the data placed on the data bus becomes the low order portion of the interrupt vector address. Interrupt processing thus starts at an arbitrary 16 bit address formed from the I register and a variable input. Another interrupt system provided by the Z-80 is called non maskable interrupt (NMI). This interrupt will occur anytime the Z-80's pin 17 is brought low, and is intended for highest priority operations like responding to a power failure before the power supply capacitors bleed down.

IC50, IC44, IC36, IC35, IC34 and IC27 provide the needed interrupt processing interfaces. The 74125s of IC34 and IC35 provide three state buffering for the interrupt address vectoring required by Z-80 interrupt modes 0 and 2. The 7442, IC27, produces an interrupt honored acknowledgement signal (if required) for use in mode 0. The INT input at the Z-80 pin 16 will be forced low whenever any interrupt input, except NMI, is brought low. Interrupts are interfaced using a 16 pin DIP socket.

One way to test out a newly constructed circuit (not necessarily the best way) is the traditional "smoke test": Turn on power and see if the circuit burns up. A far better method is to do a little thinking and careful inspection first.

Buffering

The Digital Group processor circuits are designed to drive a full complement of memory and IO. In addition, the processors are designed to operate under direct memory access as mentioned previously, and three state buffers permit isolating the processor card from its own (see figure 2) and auxiliary memory.

Sections of 8T97s IC41, IC42 and IC47 provide buffered address outputs from the Z-80 processor with each section capable of each driving 30 standard TTL loads. These drivers handle both memory and IO port addressing. DMA grant is connected to these drivers so that when a DMA is in process, the external device is given full control of the **address lines since the processor's drivers are in a high impedance state.**

The 8T97 sections used for data output, IC31 and IC32, provide the ability to drive as many as seven Digital Group IO boards (28 ports) without further buffering.

Data input to the processor is placed onto the internal bidirectional bus by two types of circuits. A pair of 74125s provides a three state noninverted buffering of memory input from a backplane bus (pins 5 to 12) which has noninverted data. A pair of open collector 7403s, IC40 and IC46, provide an inverted open collector drive of the same bus, a requirement since the Digital Group peripherals put data onto the backplane in inverted form. Notice, however, that the pin connections of the 7403 are compatible with the 74126 circuit, so if you desire to use this design with noninverting peripherals simply replace the 7403s with 74126s to change the sense of the data on the outputs of the receivers.

Memory (see figure 2) in this Z-80 processor circuit is of two types, EROM and programmable memory. The EROM is a single chip preprogrammed by the Digital Group to simplify system operation of our kits. If you roll your own software, a customized bootstrap EROM could also be used. When power is applied to the system, a "power on reset" function results, which starts the processor running at address 000 000. IC29 and IC25 decode the lowest 256 bytes of memory, resulting in a EROM chip enable condition. The EROM proceeds through its programming to clear the screen, display a message, initialize some program-

mable memory addresses, and control initial cassette reading.

Two K of programmable memory allows an extensive operating system to be entered from cassette. Sixteen 2102s are arranged as two banks of 8 integrated circuits. Which of the two banks selected (if either) is a function of decoding by IC23, IC24 and IC25, as well as the three jumper settings. The 7442 will assign the two banks of 2102s as the bottom 2 K of any one of eight 8 K blocks in memory address space.

The three jumpers permit assigning the processor's 2 K programmable memory to addresses other than the bottom 2 K. When a user wishes to add one or more Digital Group 8 K boards to his or her system, the processor's 2 K may be moved to fall above the highest address of the supplemental 8 K board. Example: A user has two Digital Group 8 K memory boards on his system. By assigning the processor circuit's 2 K to the address range of 16 K to 18 K, one memory board to 0 to 8 K, and the other to 8 K to 16 K, an 18 K system results, with all active memory in the low address range.

The EROM used for bootstrapping is a relatively slow device, so the processor must be forced to wait for its data access. A 74121 provides a 475 ns delaying pulse to the processor when either the processor EROM is accessed or an external slow memory access is required. Since the Digital Group programmable memory cards are built using 500 ns access time (or faster) 2102 static memories, the processor normally runs at full speed.

Some Notes on Construction

While the circuit diagrams of figures 1 and 2 provide the information needed to wire wrap or hand wire your own Z-80 processor, I'll bet you'll find the Digital Group processor board in our kit to be a worthwhile time saver. This Z-80 processor card is manufactured using two sided FR-10 printed circuit board material and measures 12 inches wide by 5 inches high (30.5 cm wide by 12.7 cm high). It has a dual 50 pin (100 terminals in all) connector to the backplane assembly. The definition of signals at the connector is provided in table 1.

The Digital Group board is not "Altair compatible" due to two major system constraints: processor independency and use of a single fully protected external power supply. These design goals ruled out the bus structure supported by MITS and independent suppliers of peripherals for MITS systems. Experienced designers will undoubtedly interface the Z-80 to the "Altair bus" but the processor dependency problem will remain. Some experimenters may wish to custom design this Z-80 into their own system. The circuit of figures 1 and 2 should provide sufficient details of the Z-80's operation to assist you and provide a starting point. Further detailed information on the Z-80 chip and its specifications is of course available from its manufacturer, Zilog Inc.

Testing

After building the processor circuit, but before inserting any of your (socketed) integrated circuits, try a little preliminary testing with an ohmmeter. Check for a short between backplane terminals 1 and 2, 2 and 50, and 1 and 50. 1 and 2 should show an initial momentary low resistance and then approach infinity as power supply bypass capacitors charge up. 2 and 50 will show some resistance due to the zener, and to ohmmeter polarity, but not a short.

Two techniques are possible at this point. One way (referred to in the fine print of traditional literature as the "smoke test") is to plug in all integrated circuits and insert the card in a backplane assembly wired for

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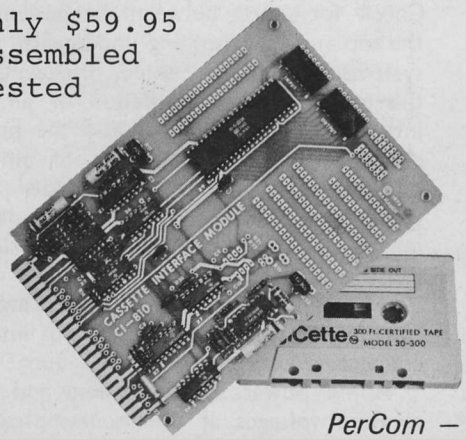

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Table 2: Power connections for the Z-80 processor circuit shown in figures 1 and 2. Note that IC8 and IC9, IC18 and IC19 are omitted from the numbering sequence.

Number	Type	+5 V	GND	−9 V
IC0	2102	10	9	–
IC1	2102	10	9	–
IC2	2102	10	9	–
IC3	2102	10	9	–
IC4	2102	10	9	–
IC5	2102	10	9	–
IC6	2102	10	9	–
IC7	2102	10	9	–
IC10	2102	10	9	–
IC11	2102	10	9	–
IC12	2102	10	9	–
IC13	2102	10	9	–
IC14	2102	10	9	–
IC15	2102	10	9	–
IC16	2102	10	9	–
IC17	2102	10	9	–
IC20	1702A	12,13, 15,22, 23	–	16,24
IC21	74121	14	7	–
IC22	7400	14	7	–
IC23	7442	16	8	–
IC24	7404	14	7	–
IC25	7420	14	7	–
IC26	7430	14	7	–
IC27	7442	16	8	–
IC28	7402	14	7	–
IC29	7474	14	7	–
IC30	8T97	16	8	–
IC31	8T97	16	8	–
IC32	8T97	16	8	–
IC33	7404	14	7	–
IC34	74125	14	7	–
IC35	74125	14	7	–
IC36	7430	14	7	–
IC37	74123	16	8	–
IC38	4010	16,1	8	–
IC39	74125	14	7	–
IC40	7403	14	7	–
IC41	8T97	16	8	–
IC42	8T97	16	8	–
IC43	Z-80	11	29	–
IC44	74LS02	14	7	–
IC45	74125	14	7	–
IC46	7403	14	7	–
IC47	8T97	16	8	–
IC48	7442	16	8	–
IC49	7440	14	7	–
IC50	7400	14	7	–

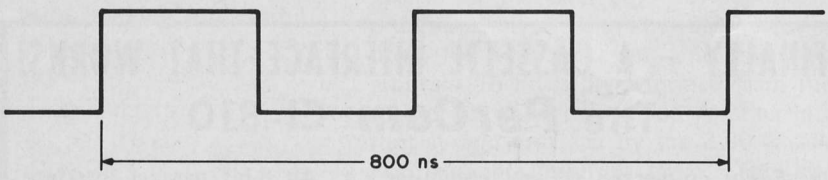

Figure 3: Central processor clock timing waveform. To verify the frequency of oscillation with a calibrated oscilloscope, measure the total time interval for two cycles of the clock waveform. This interval should be 800 ns if the correct crystal is used and it is oscillating at its fundamental frequency. A frequency counter would show 2.5 MHz as the frequency.

power. Another way is to insert only one or two integrated circuits at a time, function by function, and test as you go. The Digital Group has found a compromise which seems to work best when building kits, namely to plug in all but most critical or expensive integrated circuits, then test. This approach is optimal when using printed circuit wiring since the probability of a disastrous wiring error is in general low, assuming a fully debugged printed circuit board. Then if OK so far, plug them in and go ahead.

So, proceeding with this approach, insert all integrated circuits *except* the Z-80, the 1702A, and the 2102s. Note that all integrated circuits except 2102s in the Digital Group Z-80 board have their keyway or dot indicating the pin 1 end oriented away from the connector.

Measure the resistance at the backplane voltage supply pins again. In particular, note the lower resistance value between backplane pins 1 and 2. Reverse the ohmmeter and remeasure. A shorted reading now indicates a bad integrated circuit, and near equal readings indicate a reversed integrated circuit somewhere. Now insert the crystal into its holder. In our Digital Group kits this is done by snapping in the body of the crystal (gently), then pushing forward to contact the pins.

Before inserting the processor card into its backplane connector, measure the voltages at the connector. A single wrong voltage may cost you a board's worth of ICs.

Measure these backplane pins against ground:

Pin 1 – +5 V ±5%
Pin 2 – 0 V
Pin 50 – −12 V ±10%

(The backplane pin 1 end is marked on the Digital Group Z-80 processor card. If you use a homebrew assembly, use the equivalent test before proceeding.)

Make a final inspection of the processor. Check for shorts between components on the top and lines running underneath. In kit systems, look for any solder bridges. Check the proper pin 1 orientation of all your integrated circuits. If you use the printed circuit, sight down the rows of pins for missing solder points. Missed solder points typically seem to occur at the end pins of integrated circuit sockets, and one side of resistors or capacitors.

After all this preliminary checking you can insert the processor board into its connector.

Apply power to the system and again measure voltages at the processor card as noted previously.

Checking Your Waveforms

Connect a calibrated triggered sweep oscilloscope to pin 6 of the 7400 IC50b. Set the triggering to occur on the positive edge, and the sweep setting to 100 ns per division. Look for a two cycle time of 800 ns seconds as shown in figure 3. If your oscilloscope does not sweep as fast as 100 ns/div, then a slower sweep can be used; but be absolutely sure that the two cycle time is exactly 800 nanoseconds as shown in figure 3.

A frequency counter may also be attached to pin 6 of IC50b. The desired frequency is 2.5 MHz. Any appreciable error indicates either a defective crystal, a bad 7400, or an overtone oscillation (one way to correct this last case is by using 74L00 for IC50).

Measure the voltage at the following pins (before expensive integrated circuits have been inserted). Correct any discrepancy.

Z-80 (IC43)	: pin 29 = 0 V pin 11 = +5 V
1702A (IC20)	: pins 24 & 16 = –9 V pins 12, 13, 15, 22 and 23 = +5 V
Any 2102 RAM:	pin 9 = 0 V pin 10 = +5 V

Carefully insert the Z-80, the 1702A, and the 2102s. With the large Z-80 and 1702 circuits, insertion should be done evenly without allowing excessive stress. Packages have been known to crack into two parts during insertion. Make sure that pin 1 (indicated by either a dot or a 1 on these circuits) is properly oriented. Recheck the processor circuit asembly for orientation, lead shorts, solder shorts, and missing solder joints. Think courageous thoughts. Plug in the processor board. Bravely turn on power.

Using the Z-80 Processor Card

Several operational systems structures (see my June 1976 BYTE article) are consistent with this processor circuit design. This Z-80 circuit can be used with a minimal amount of additional hardware (a PIA and UART, a Teletype machine, and a suitably programmed EROM) as if it were an "evaluation board" that maintains system dependency so that different processor integrated circuits may be compared.

Preferably, this board becomes the key component in a much larger general purpose system. A special EROM is provided in the Digital Group Z-80 kit which interfaces this Z-80 board to our audio cassette and TV based system structure. A cassette of programming is provided with our kit version, which loads programmable memory with an operating system for reading and writing cassettes, and building and displaying programs.

Conclusion

The Z-80 is a neat chip to use. Contrary to some grapevine rumors, you can't simply unplug your 8080 integrated circuit and plug in the Z-80; but it is an architecturally simple chip to design with. I hope this design excites you as much as the Z-80 excited me. Enjoy.■

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