the digital group
po box 6528 denver, colorado 80206 (303) 777-7133

FLOPPY DISK DOCUMENTATION

298-075-B-44+2+69

CUSTOMER UNPACKING INSTRUCTIONS FOR THE SHUGART FLOPPY DISK DRIVE

Before this drive can be operated, a block of foam must be removed from the drive mechanism. This foam keeps the head and plastic load pad arm separated during shipping. The drive electronics board is exposed and should be inspected before operation. Check to see if the jumpering (shorting plugs) are in place, according to Figure 3. An additional wire connection is made between J1 and J5 to connect -5V DC provided by the CPU cabinet to the DC power block, J5. Pins 2 and 4 on the drive electronics board are designated -5V DC. Solder a piece of insulated wire (approximately 18-24 gauge) between pins 2 and 4 on connector J1 and pin 4 on connector J5 as shown in Figure 3. Information on loading diskettes, operating the drive, user options available, and power supply connections are illustrated in the drive manuals included. Be careful not to damage traces or remove traces on the drive electronics card when making user options or when connecting power.

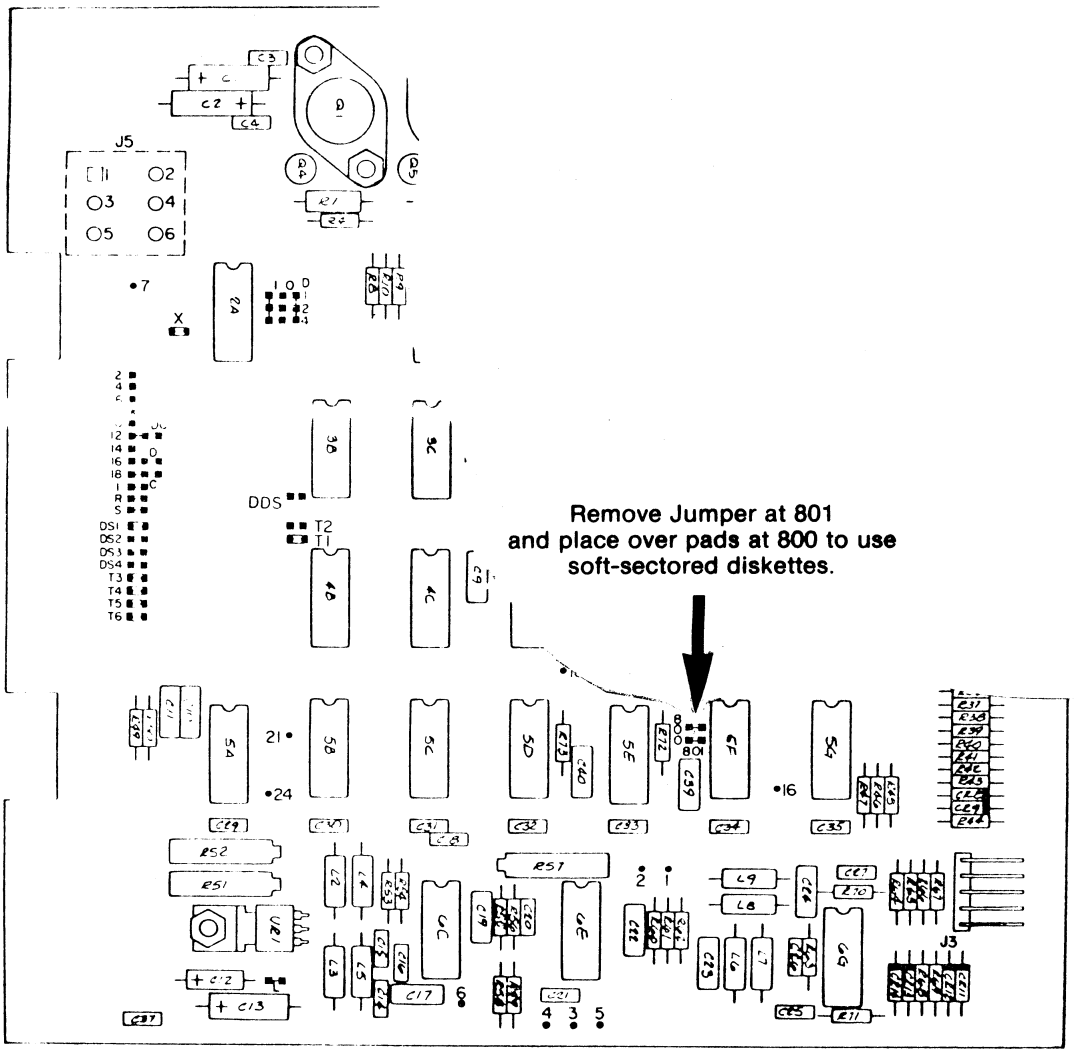
Be sure that the drive connector is properly connected to the drive electronics board connector, J1. The label on drive connector pin 2 must face pin 2 on drive electronics board connector J1. Reversing this cable may cause damage to the drive by applying voltage to an incorrect pin.

The drives come from the factory with shorting jumpers installed as shown in Figure 20 in the Shugart OEM manual. The drive select shorting block should be placed on the appropriate drive DS1 - DS4. For a one drive system be sure that the shorting plug is installed at DS1 (see Figure 3), drive select 1. Jumpers are also installed on the terminator posts T3, T4, T5, and T6. Remove these shorting plugs from all drives except the last one on the interface. Using Figure 3, install jumpers at pins C, Z, and DS. This should be done by removing plugs from pins X, Y, and HL and installing them on pins C, Z, and DS, respectively.

The Drive will presently use hard-sectored diskettes only. To modify the Drive electronics board to accomodate soft-sectored diskettes, a shorting plug must be installed across the set of pads labeled *800* on the drive electronics board as shown below. Remove the shorting plug from the set of pads labeled *801* and place across the set of pads labeled *800*.

All other jumpers should remain as installed. If any questions or problems arise, please contact The Digital Group or a Digital Group dealer.

Three Shugart manuals—OEM, Theory of Operation and Maintenance—have been reprinted by permission of Shugart and provide useful information on installation and operation of the Shugart disk drives.



▪▪ Jumper Plug Installed as Shipped

• Test Point

SA800/801 PCB Component Location

Soft - Sectored Disk Jumpering — SHUGART

CUSTOMER UNPACKING INSTRUCTIONS FOR INNOVEX FLOPPY DISK DRIVE

Before this drive can be operated, two pieces of foam must be removed from the drive mechanism. Orient the drive so that the black side of the cabinet is facing up. The hinged black plastic door, where the floppy disk is inserted, should be facing you. On the left side of the bronze colored casting are two screws which hold this black lid closed. These must be unscrewed (backed out) sufficiently to enable the black cover to swing open on its hinges. The cover will swing up and lock open.

A small piece of grey or black foam will be seen resting between the rail and the white plastic load arm lifter. Remove and discard this foam being careful not to misalign the solenoid clapper assembly.

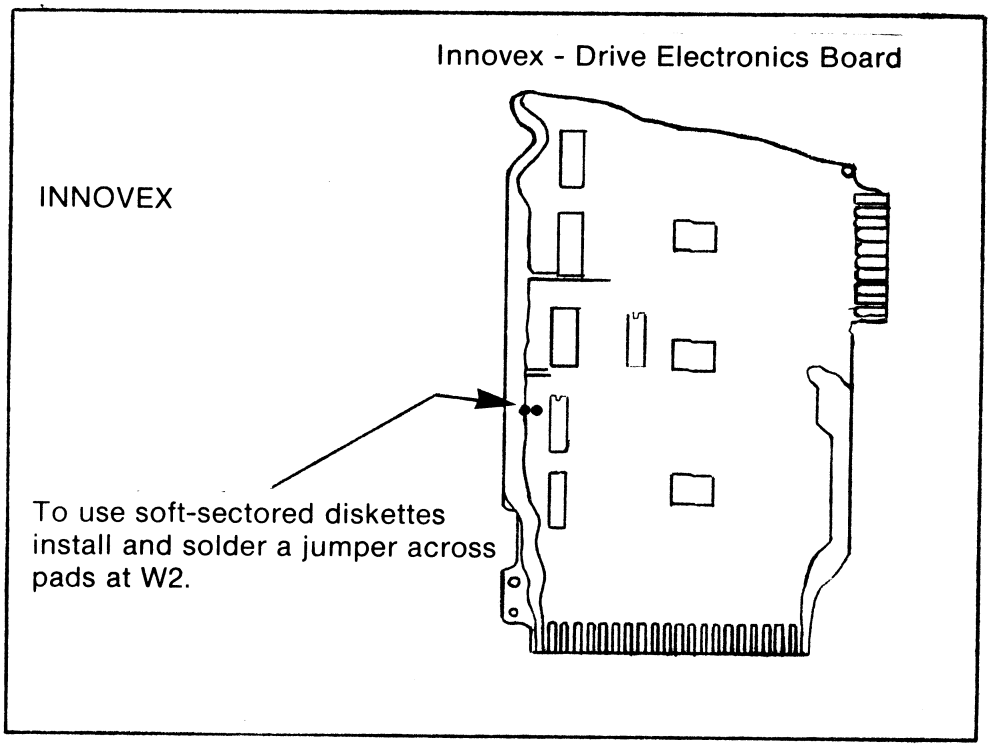
On the back side of the drive is a black canister which is the stepping motor housing. Projecting from the center of this housing is a steel shaft extension. Using the shaft extension, turn the screw until the carriage is against the front stop. Remove the foam block from the "V" shaped cavity in the web of the base at the rear of the unit.

Again using the shaft extension at the rear of the stepping motor, turn the screw until the carriage is against the rear stop.

Now close the black lid and lightly tighten the two screws which you loosened to open the lid.

The Drive presently uses hard-sectored diskettes only. To modify the Drive electronics board to accomodate soft-sectored diskettes, install a jumper wire on the Drive electronics board at the trace labeled W2.

Soft - Sectored Disk Jumpering — INNOVEX



Floppy Disk Controller Card

Introduction

The Digital Group now offers all the capablilities of rapid access mass storage. With the addition of a floppy disk subsystem, the Digital Group system user can now have at his disposal 256K to 315K bytes/disk in IBM compatible format, with a worst case access time of one second.

A fully operational Digital Group floppy drive system is based on a Digital Group computer with a recommended memory size of 26K and a Z80 or 8080 based processor. The complete floppy disk subsystem has a floppy disk controller card, one to four drives, power supplies for the disk drive, necessary cabling and system interconnect wiring, and cabinet(s).

The controller card uses a standard I/O slot on the Digital Group bus (one 36-pin dual connector and one 22-pin dual connector). The voltages required by the controller card are +5V DC @ .9 amps, +12V DC @ 35 ma, and -5V DC with negligible current drain, and are supplied by the I/O bus. The voltages required by a standard drive are +5V DC @ 2.5 amps, +24V DC @ 1.4 amps and 115V AC @ .2 amps, all supplied by the separate power supply of the disk drives, and -5V DC @ 75 ma, supplied by a Digital Group system through the CPU cabinet backplane. The disk cabinets provide housing for one to two drives plus the power supply. Assembled cabling is provided for connection between all system components when a complete system is ordered. .

The controller card which interfaces between the micro computer and disk (and associated drive electronics) utilizes a floppy disk controller chip which handles all READ and WRITE operations to and from the disk. Other components on the controller card provide the proper timing, buffering, signal conditioning and addressing circuitry to support the controller chip. The card is compatible with IBM 3740 as well as other formats. It provides programmable track stepping rates, programmable sector sizes, and changeable data transfer rates. The card generates CRC error detection code,and initializes and formats diskettes. It will also use hard-sectored or soft-sectored disks. One controller card will support up to four standard drives and can also be used to interface with mini-floppy drives. The controller card requires jumpering to select a group of seven sequential port addresses that are used to address the card. Standard jumpering as detailed later in the assembly instructions selects ports F0 - F7.

The software listing initially supplied with the disk includes the drive handling routines that control sector reading and writing, and track seeking operations. A disk operations system is presently being written to provide full disk support.

The addition of disks in a Digital Group system requires slight modification to the CPU card to provide synchronization between the disk and the processor for READ and WRITE operations. And the power on reset from the CPU card (pin 47) is used to reset the controller chip as well, and requires a jumper cable. Complete assembly is detailed in later steps.

SYSTEM DESCRIPTION

The controller card is the interface between the CPU and the floppy drive(s). The controller card documentation includes a complete technical description of the controller card and controller chip, assembly instructions (including CPU card modifications), software description, listing, and tape, and diagnostic testing procedures.

To complete your floppy drive system, several additional items are required. These items are all included when ordering a complete system and may be purchased seperately from The Digital Group at any time.

1. **Power Supply.** Each drive requires both AC and DC power sources as shown in Figure 1. AC connections for each drive are supplied with the drive. DC connections (+24V, 24V ground, +5V, 5V ground) to each drive are provided with the Digital Group floppy power supply. Be sure all power sources are properly fused and grounded. Complete documentation is provided with each power supply.

2. **Cabling.** Cables from the controller card 36-pin connector to the floppy drive(s) 22-pin connector(s) are required to transfer the proper signals. Figure 2 details the pinout of the floppy disk controller card 36 pin connector. Figure 3 (one each for Innovex and Shugart drives) details the pinout of the floppy drive connector. Included in the standard Digital Group cable-pack are Molex connections from the back of the motherboard to the CPU backplane and a flat cable from the backplane to the drive(s). A different cable-pack is required depending on the number of drives in your system and an upgrade kit is available if you add drives at a later date. Complete documentation is provided for cabling your system with each cable-pack.

3. **Drives.** Floppy disk drives are available in standard or mini format from Innovex and Shugart. Up to four drives may be used with the floppy controller card. Each drive includes a short AC line for connection to a power source and a complete technical manual from the drive manufacturer.

4. **Cabinets** that match the rest of your Digital Group system will be available for single or dual drives in both standard and mini formats. Each cabinet has space for two drives and a power supply. Cabinets include AC line cord, fan, and switch, as well as assembly documentation.

AC AND DC WIRING DIAGRAM

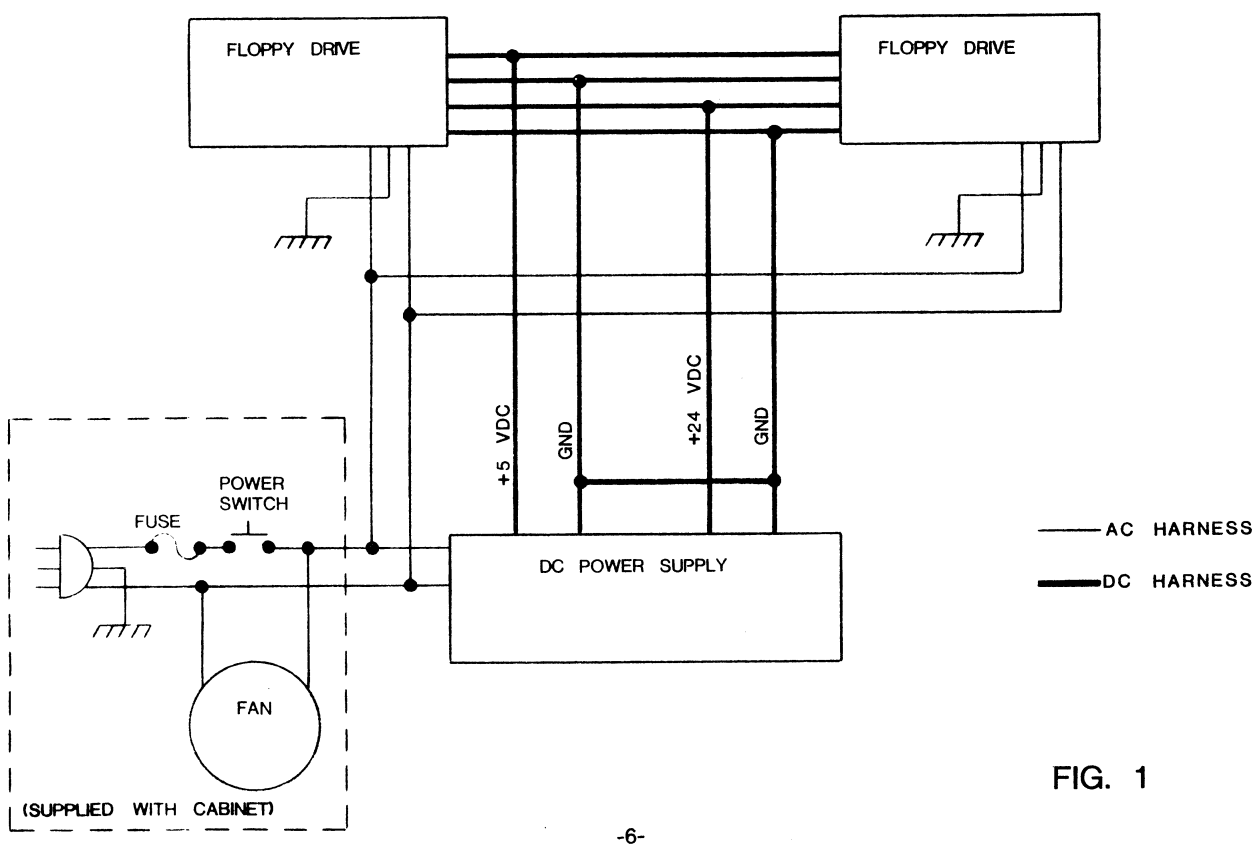


FIG. 1

FLOPPY CONTROLLER CARD, 36-PIN CONNECTOR, PINOUT

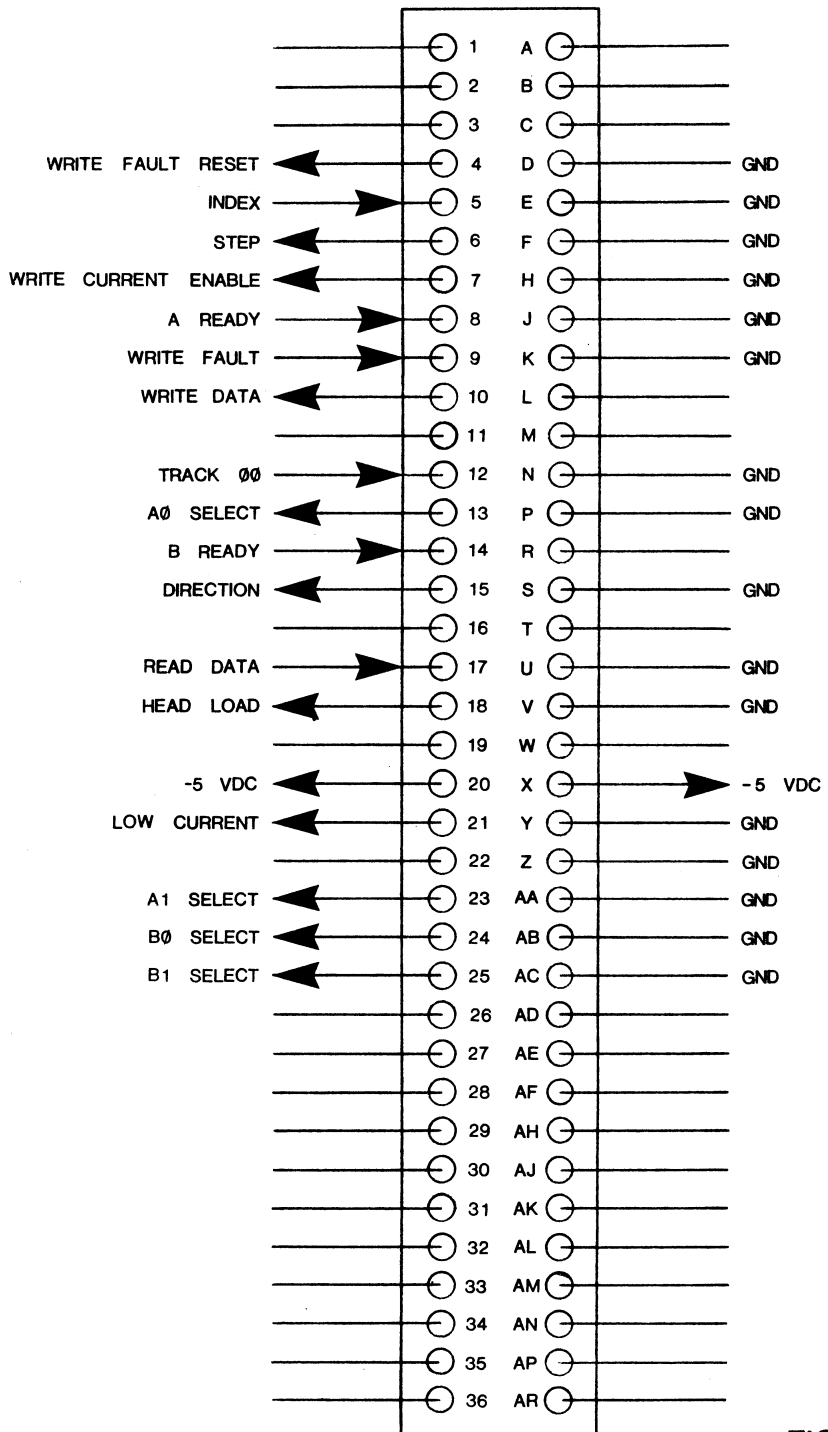
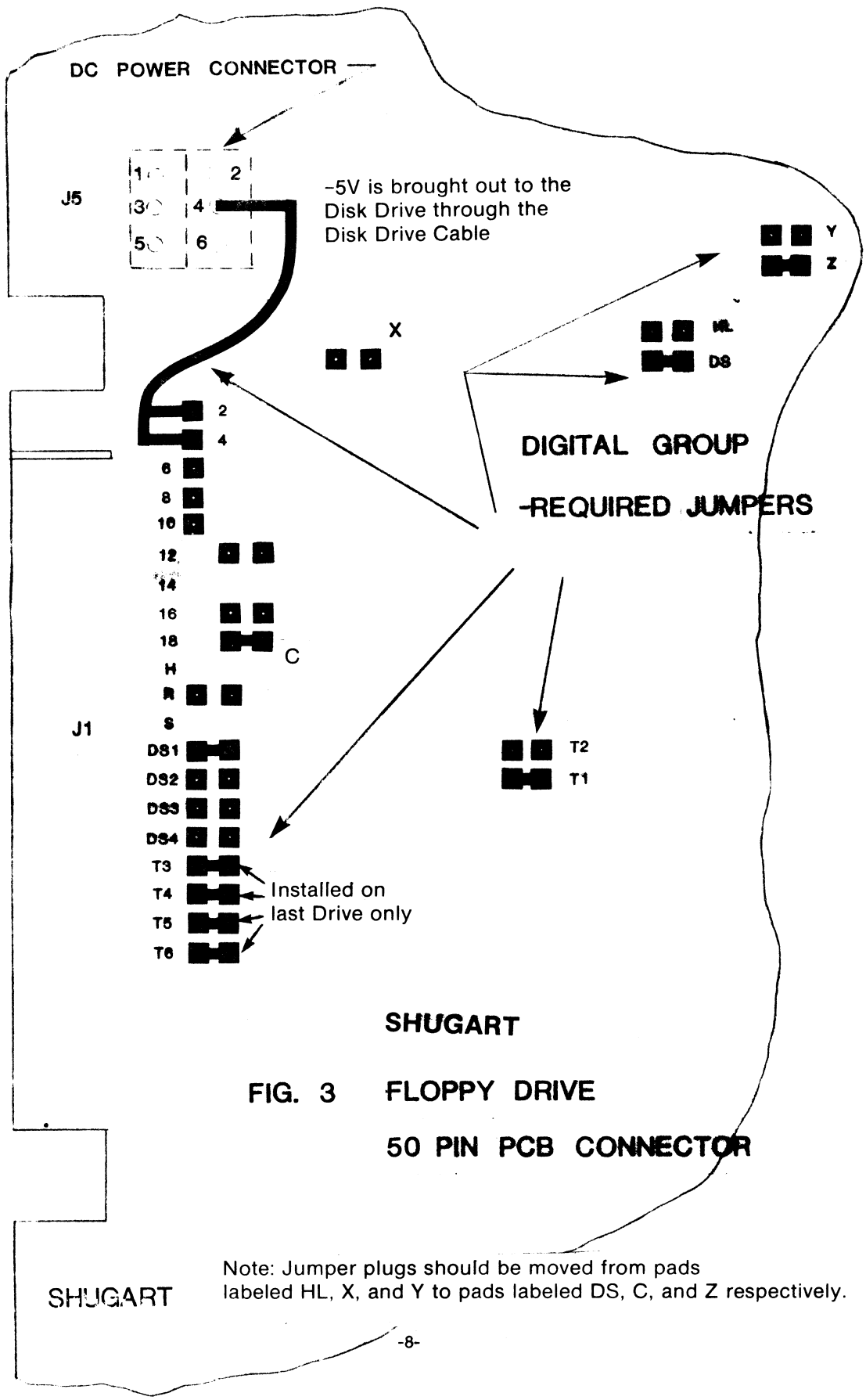


FIG. 2


DC POWER CONNECTOR
J5
1
2
3
4
5
6
-5V is brought out to the
Disk Drive through the
Disk Drive Cable
Y
Z
X
HL
DS
2
4
6
8
10
12
14
16
18
H
R
S
C
J1
DS1
DS2
DS3
DS4
T3
T4
T5
T6
Installed on
last Drive only
T2
T1
DIGITAL GROUP
-REQUIRED JUMPERS
SHUGART
FIG. 3 FLOPPY DRIVE
50 PIN PCB CONNECTOR
SHUGART
Note: Jumper plugs should be moved from pads
labeled HL, X, and Y to pads labeled DS, C, and Z respectively.

FLOPPY DRIVE 22-PIN CONNECTOR PINOUT (INNOVEX)

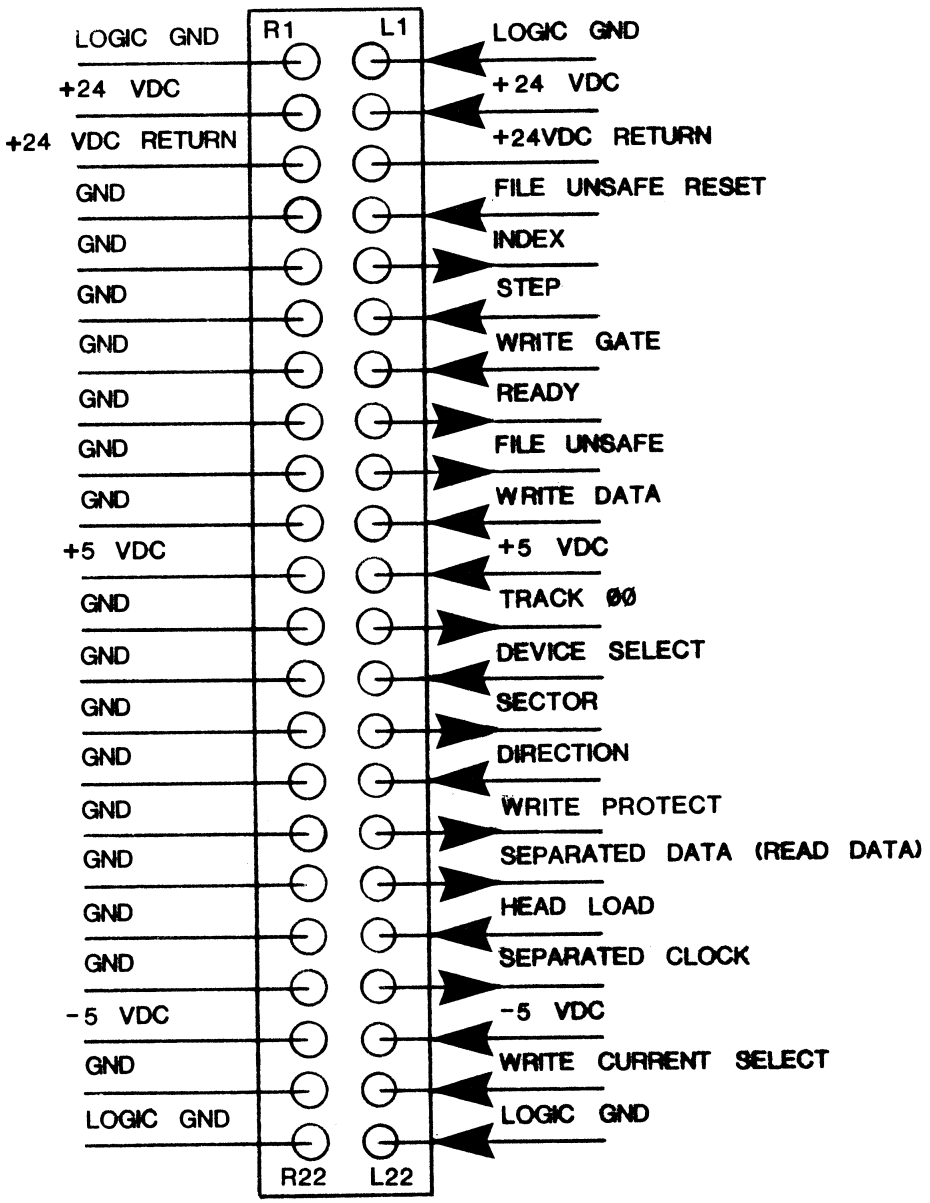


FIG. 3

Technical Description — Floppy Disk Controller Card

The purpose of the card is to record and reproduce information from a floppy disk drive. The format of that information is standard IBM format (soft-sectoring), although other formats are possible. Information is stored serially on tracks on a magnetic medium — the diskette. The card serves as an interface between the disk drive and the CPU.

The heart of the card is an NEC uPD372D floppy disk controller chip. Conceptually, the chip is a collection of latches or registers holding information received from the disk or the processor to be transferred onto the disk or used to control the drive. The chip converts serial data to 8 bit bytes to send to the CPU and also converts parallel information (bytes) to serial data for writing on the disk. The chip handles all the formatting required and contains a cyclic redundancy check generator or CRC generator for detecting read or write errors. The rest of the circuitry on the controller card provides the proper timing signals, buffering and support for the chip.

The controller chip is IC4 on the schematic. To its right are the control lines going to the disk drive. IC5 and IC7 are buffers which also invert the active high logic of the controller chip to the active low logic of the disk drive. IC2 (hex Schmitt trigger package) eliminates or reduces noise from the disk drive signals coming into the controller chip and also inverts the logic to the chip. Data to be written on the disk leaves pin 18 of the controller chip and is formatted and presented in proper form to the disk by IC3 and IC9.

Data read from the disk enters at pin 17 of the card. The network of IC6, IC13, IC10, IC8, and IC11 separate the raw data from the disk into data and clock pulses. The recording format of the disk consists of clock pulses interspersed with data pulses. The clock pulses occur at a fixed rate. To record a "1" between clock pulses, a data pulse must occur between the two clock pulses. If no data pulse occurs between the clock pulses the chip will know that a "0" was recorded. This method of recording and recovery incorporates self-clocking into the circuitry so synchronization is maintained between the data recovery circuitry and the information coming in from the disk. Information is received by the controller chip as separated clock and data pulses.

The controller card incorporates an 8224 clock generator and driver that produces high level clock signals for use by the controller chip. A frequency countdown chain of IC14 and IC16 form a write clock signal which is input to the controller chip at pin 13. On-board jumpering provides an extra stage of frequency countdown to allow card operation with mini-floppy disk drives. Mini-floppies differ from standard disk drives in that they have half the data rate, half the storage capacity and double the head settling time of a standard drive.

The circuitry to the left of the controller chip on the schematic interfaces the chip with the bus environment of the CPU via the I/O bus. IC22, IC25, IC31, and IC28 buffer the signals between the I/O bus and the controller chip. The port address lines of the controller card can be classified into two groups. A3-A7 (pins S, T, U, V, and W) enter a decoding network of port select jumpers and IC32, and serve to address the card. The controller card with the present software requires jumpering to sequential I/O ports F0 thru F7 hexadecimal. A0-A2 (pins N, P, and R) are used to address the internal registers contained in the controller chip. The controller chip contains six registers for transfers to the disk and three registers for transfer of information to the CPU. The register select lines, A0-A2, enter the card and are latched into IC29. The register address is then held long enough by the latch circuitry to allow an accurate transfer to occur with the selected register.

When A0-A2 are all "high", a register which is not internal to the controller chip is selected. IC27 decodes this register selection as a data request from the CPU. This "port 7" address, when gated with a WRITE signal from the CPU, sets up a one-shot, IC11 (74123), which generates a CPU WAIT signal. The one-shot pulse length is set to be greater than a single disk revolution time so that the controller chip will synchronize data transfer with the CPU. The controller chip samples input data from the disk, looking for an address or data mark. When the controller finds the proper data pattern, it sends back a data request pulse though IC19 that clears the one-shot, IC11, and clears the WAIT signal it was posing to the CPU. IC19 also clears out any triggers to IC11 that may occur when initially turning on power to the disk or during any front panel reset operation. This allows the CPU to run until the controller chip is ready to transfer information. Note that the controller card requires an input to the WAIT line on the CPU card and a RESET line common with that on the CPU card.

$\overline{\text{READ}}$ and $\overline{\text{WRITE}}$ signals from the CPU enter the controller card on pin 11 and pin X on its 22-pin connector. A $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ signal along with a controller card SELECT signal from IC32 pin 2 is gated in IC26 and clocks IC20. IC20, IC24, IC18, IC19, IC15, IC12, and IC16 form a state generator which contols the proper sequence of data being entered or taken from the controller chip. The state generator remembers which operation occurred last, and for each operation provides proper timing, i.e., holding data stable and providing proper clock edges to process data. IC17 clocks the bit shift register formed by IC15, IC12, and IC16 on the lower middle half of the schematic. During a read operation it is necessary to synchronize the termination of the read cycle with the termination of the CPU READ signal. For a write operation, information is presented to the controller chip and written into internal registers and the controller chip terminates the cycle.

During a write operation IC15 (pins 2, 3, and 5) and IC15 (pins I2, 11, and 8) clock through a zero bit and delay the internal register latching into IC29 (74175) by one half clock cycle. Pin 8 of IC15 latches the address of the internal register by clocking IC29. One half clock cycle later pin 8 of IC12 sends a data strobe signal through IC10 to the controller chip which enters information on the data bus. This set up and data hold time assures that the register address and data bus are stable when a data strobe is present on the controller chip.

During a read operation IC13 pin 8 detects the end of a READ signal from the CPU. The output of IC13, also connected to the data strobe line in the controller chip, assures that data from the controller chips registers will be valid until the CPU has ended its read cycle. When the read cycle ends, IC26 pin 6 clocks IC12 pin 3 which resets the shift register chain and removes the data strobe from the controller chip through an input to IC13 pin 9. The shift register chain is reset at the end of both read and write operations and allows another cycle to occur.

The circuitry of IC20, IC18, IC24, and IC19 differentiate between the two operations. IC19, a cross-coupled flip-flop, remembers the last operation entered. When the controller chip requests a data transfer it posts a data request signal from pin 17 of the chip to IC18 pin 11. The data request signal also clears the CPU WAIT signal, allowing the CPU to run. The posting of the data request bit must be removed by the setting of a bit in an internal register. There is not an external data request reset signal. The circuitry to the immediate left of IC29 hardwires the register address and the appropriate bit to reset the data request signal. This reset operation is automatically initiated when a data request signal is clocked into IC18 pin 11. IC19 pin 1 latches this hardwired information in IC29. A READ or WRITE signal to the card is sensed by IC26 pin 3 and IC20, and IC18 initiates the operation of the state generator, i.e., sending a "0" bit through the chain of shift registers for each operation cycle. The order in which IC18 and IC20 are toggled determines the state of the cross-coupled flip-flop output, IC19. IC19 serves to differentiate between the cycles and remembers which cycle is being activated through the shift registers. At the end of the cycle IC18 pin 2 and IC20 pin 2 will receive the cycle that just ended from IC19 and will only reset the cycle last initiated.

Assembly Instructions

The recommended procedure for installing and operating the disk in a Digital Group system is detailed briefly below, with more explanation and figures provided in later documentaion.

Steps

1. Assembly of Disk Controller Card
   a. Component assembly
   b. Port jumpering

2. CPU Board Modification—(Z80 CPU card detailed)
   a. Cutting one trace
   b. Adding two diodes (1N4148)
   c. Adding jumper wire to pin BC—CPU card
   d. Addition of CPU WAIT line wire—from controller card (pin 36) to CPU card (pin BC)
   e. Addition of reset jumper from controller card (pin 35) to CPU card (pin 47)

3. Cabling Procedure—complete documentation supplied with cables
   a. Addition of Molex jumpers from controller card (36-pin dual connector) to unused CPU backplane connector (22-pin dual connector)
   b. Installation of cable from CPU backplane to drive
      1) Drive select jumpering
      2) Ohmmeter testing of controller—drive connections
   c. Hook-up of power supply to drive connector and testing without the drive connector installed on drive.

4. Perform diagnostic testing with drive connector installed as described in the software section of this documentation

Construction

Estimated Construction Time: 3-5 hours

To build The Digital Group controller card you will need the following tools and equipment:

Fine-tipped low wattage soldering iron (approximately 25 watt)
Solder--60/40 resin wire solder, 20 gauge (approximately)
Do not use acid core solder!
Diagonal cutters--small micro sheer type preferred
Long-nosed pliers
Screwdriver
Flux remover or alcohol
Small brush

Before beginning to mount and solder components inspect the controller card. The side from which the components are mounted is labeled "Floppy Disk Controller" on the middle bottom portion of the board. Compare the areas where IC sockets will be inserted with the layout to see that there are no shorts occurring between either the traces leaving the IC or the IC pads or holes in which the IC's are mounted. While plating errors like this are a rare occurrence and The Digital Group tries to inspect and maintain the quality of its printed circuit boards, once the IC sockets are inserted it is very difficult to find such a problem.

Next, identify the components that will be used on the controller board. The most difficult task is generally identifying capacitor values and types of capacitors. All resistors have standard color code markings bearing the value and tolerance of the resistor. The parts list calls for 1/4 watt and 1/2 watt resistors. Disk capacitors may be identified in general by their disk-like shape and usually by their ceramic covering. Note that the operating voltage specified for capacitors is the minimum acceptable rating. Capacitors supplied with specific boards may have a higher voltage rating than called for in the parts list but should be used despite the variance, and will not affect the circuit operation. Mica capacitors may be identified by a slightly wider lead spacing and a more rectangular shape.

Electrolytics generally come in tubular casings and should be clearly marked with the polarity indicated by a "+" on one end or by arrows indicating polarity.

Tantalum capacitors have a polarity which is indicated by a leg which is a different color than that of the capacitor body or by a "+" marking. When installing capacitors on the board, match the polarity of the capacitor with the screened label on the board.

Finally, when beginning construction of the controller card it is important to have a clean working area that is well lighted and ventilated since these conditions can affect the quality of your assembly. Also, make sure that your soldering iron tip is hot enough, is kept tinned, and is cleaned periodically with a sponge or similar material.

Most problems that arise with newly assembled boards are related to either solder shorts or splashes, improperly soldered joints ('cold' solder joints) or missed (unsoldered) pins. Properly soldered joints are shiny and solder on an IC socket should extend slightly from the pad or socket hole to the component lead or pin. All IC's are socketed on The Digital Group boards so the sockets may be installed prior to mounting IC's to avoid damaging the heat-sensitive IC's.
NOTE: Probably the second largest problem with newly assembled boards is incorrectly installed parts (polarity, pin orientation, etc.) or wrong-valued parts being installed.

01. ☐ Begin construction by inserting all IC sockets on the component side of the board according to the layout and parts list. Sockets should be held closely against the board while soldering. Two techniques may be used:
    1) Individually mount and solder each socket, placing any socket orientation away from the bottom of the board (the edge with the two connectors), or
    2) Insert all sockets and, using a rigid piece of material larger than the controller card, hold the sockets against the board while the controller card is inverted and soldered.

02. ☐ Next, insert the 17 resistors (R1-R17) according to the layout, the parts list, and lead spacing on the board. Resistors and components in general should be mounted as close to the board as possible. Extended leads on discrete components will increase system noise and have other effects on system operation. Mount components such as capacitors or diodes so that descriptive labeling may be read when inspecting the board.

03. ☐ Insert and solder the silicon diode, D1. The diode should be oriented with the cathode (the end marked by a bar) mounted toward the right.

04. ☐ Insert and solder the 29—.01 mfd ceramic disk capacitors C1, C2, C4, C6, C10-C14, C17-C20, C22, C24, C26-C30, C32-C39, C41. There is no polarity to be observed for their installation.

05. ☐ Insert and solder the mica capacitors C3, C5, C7, C8, C9, C15 and C21 as shown on the layout. Again, no polarity is to be observed when installing mica capacitors.

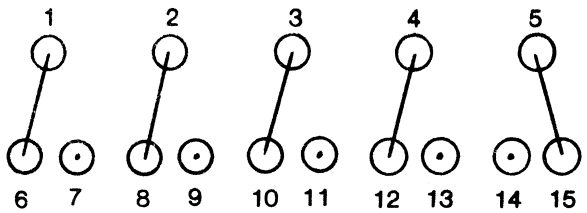
06. ☐ Insert and solder the tantalum capacitors C23, C25, C31, and C40, noting the polarities indicated on the capacitors, on the layout, and on the printed circuit board. The tantalum capacitors are identified by their narrow lead spacing, balloon-shaped casing and the labeling on the casing.

07. ☐ Insert and solder the electrolytic capacitor, C16, noting its polarity and wide lead spacing.

☐ Install the 18 MHz crystal socket without the crystal in place. Trim the crystal socket pin to fit into the proper holes as indicated on the layout and also press the rear tab of the socket into the place provided on The Digital Group board.
NOTE: Crystals are heat sensitive and may be damaged by direct installation and soldering into the board. Avoid applying heat to the crystal by use of the flat crystal mount.

09. ☐ Install the 18 MHz crystal (Y1).

10. ☐ The last construction detail is providing jumpering for I/O port selection on the board, and for drive type (standard or mini drives). With Innovex or standard drives and with available software for the card, the jumpers should be installed as shown below using the wire supplied, or wire of approximately 28 gauge.



PORT SELECT JUMPERS

11. ☐ Begin preliminary testing of the card. Measure the resistance between ground (pin 2 of the 22-pin connector) and voltage supply pins 1, 20 and 22 of the 36-pin connector on the card. A very low resistance indicates a bad capacitor or a solder short somewhere on the board.

12. ☐ Next, insert all of the IC's according to the layout except for the 42-pin IC4. Pin 1 of each IC should be oriented in the upper left corner of each socket away from the connector edge of the board. Be careful not to bend pins under the socket body.

13. ☐ Make a resistance check between pins 1 and 2 (of the 36-pin connector). Measure first with the ohmmeter leads polarity in one direction and then with the opposite lead polarity. Note the values. A very low reading usually indicates a bad IC, and nearly equal readings indicates a reversed IC.

14. ☐ If you have not already done so, install a 36-pin and a 22-pin dual connector in the I/O slot where you intend to use the controller card.

15. ☐ Next, plug the board into the I/O slot of your computer, turn on power to the computer, and measure the voltage at pins 40, 39 and 21 of the IC4 socket (without IC4 installed). They should measure +12, +5 and -5, respectively.

16. ☐ Disconnect power and plug in IC4, the uPD372.

Problems occurring with newly assembled boards are usually due to solder shorts, incorrect component values, unsoldered pins or leads, or bent pins on IC's. Most IC's are static sensitive and reasonable care should be exercised when handling or transporting them. If other problems or questions arise during assembly, please call The Digital Group or a Digital Group dealer for assistance.

CPU Modification

The installation of a floppy disk and controller card in the Digital Group system requires slight modification to the CPU card itself. Since the controller card must synchronize its operation with the CPU, the controller card sends a signal (CPU WAIT) to the WAIT line on the microprocessor chip (pin 24 on the Z80 CPU chip). This line from the controller card runs to the CPU card and makes connection on a previously unused pin on the CPU bus (pin BC on the circuit side of the CPU board). See the Digital Group Systems Documentation for CPU bus pin description. From pin BC a jumper wire is connected to the existing WAIT line circuitry via one diode. Essentially, then, the circuitry change is implementing a wired OR gate to the input of IC28 (NOR gate) as shown in Figure 4

Procedure for CPU Modification

1. ☐ Identify pin BC on the circuit side of the CPU board (4th pin from the end).

2. ☐ Cut one trace connecting IC21 pin 6 and IC28 pin 12. See Figures 5 and 6.
   a. Locate trace on circuit side of CPU card matching the figure.
   b. Cut the trace between points A and B with a sharp tool like a razor blade or Exacto knife.

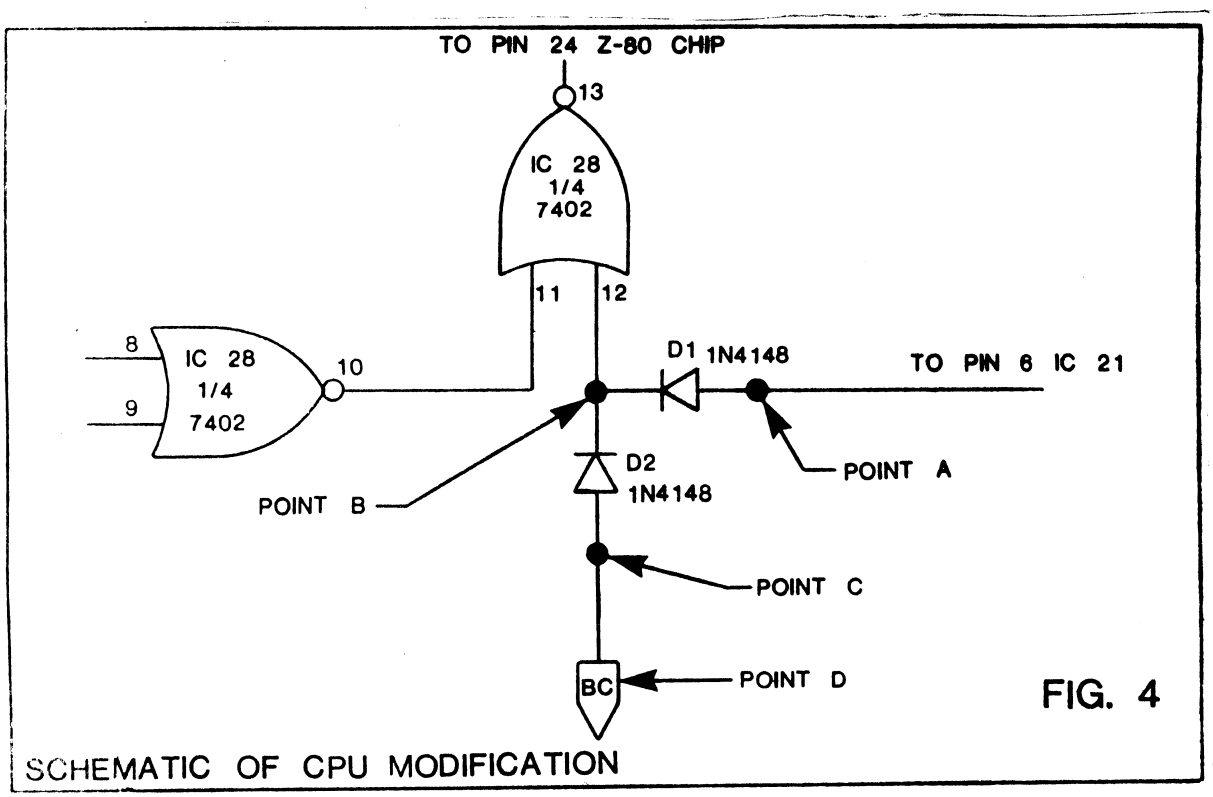
3. ☐ Solder DI (1N4148) across points A and B. The banded end of the diode should be connected at point B.

4. ☐ Solder one end of D2 (1N4148) to point B (also the banded end), leaving the point C end of the diode unconnected.

5. ☐ Cut a 6" piece of insulated wire from the wirewrap wire supplied or from #20-30 gauge insulated wire and solder it between pin BC on the CPU connector (point D) and the unconnected end of D2 (point C).

6. ☐ Add a jumper wire from the CPU edge connector (pin BC) to the controller card edge connector (pin 36) CPU WAIT line. See Figure 7.

7. ☐ Add a jumper wire from the CPU edge connector (pin 47) to the controller card edge connector (pin 35) RESET line. See Figure 7.



CONNECTION POINTS FOR CPU MODIFICATION

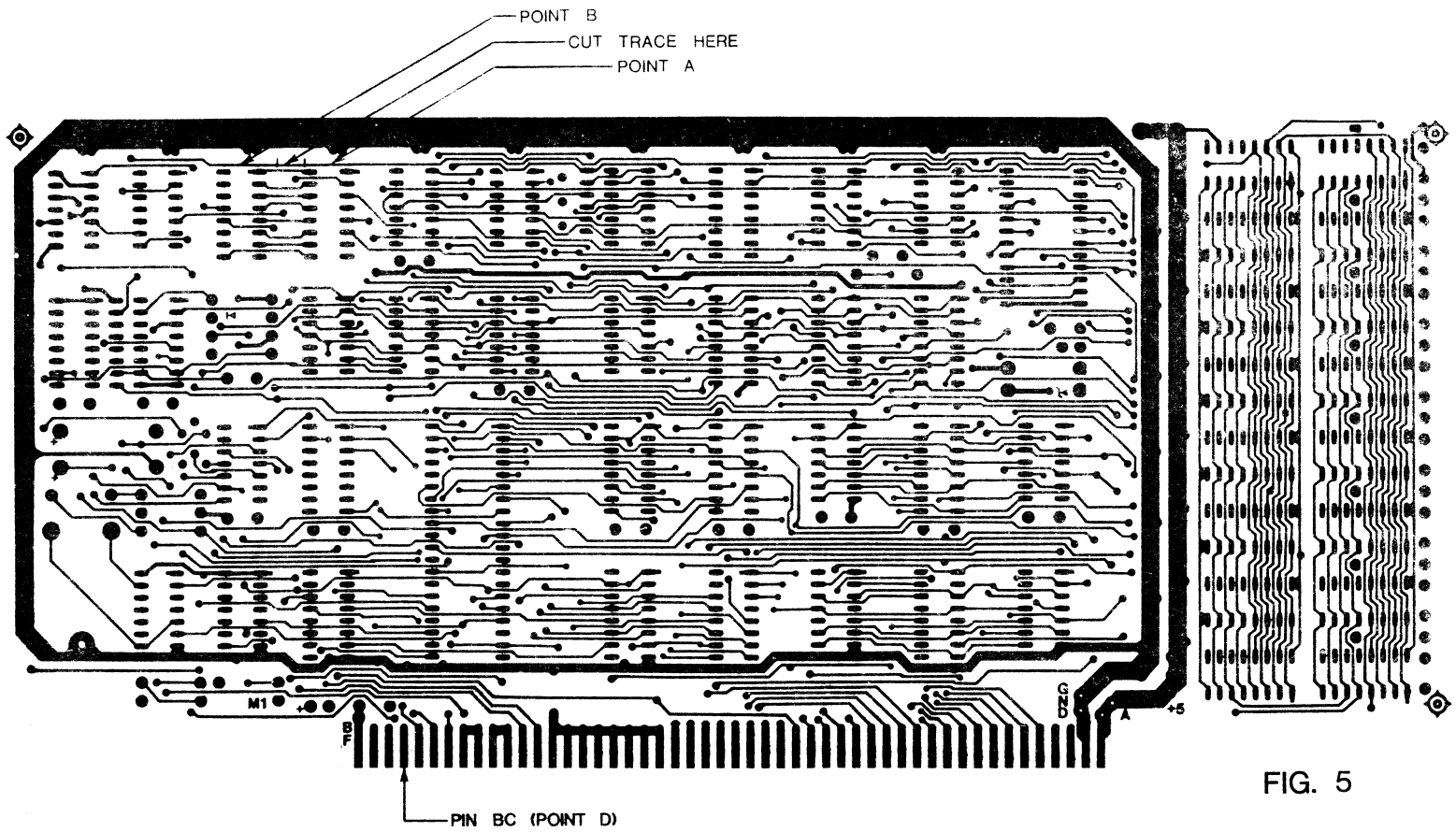


FIG. 5

CIRCUIT SIDE OF Z-80 CPU CARD

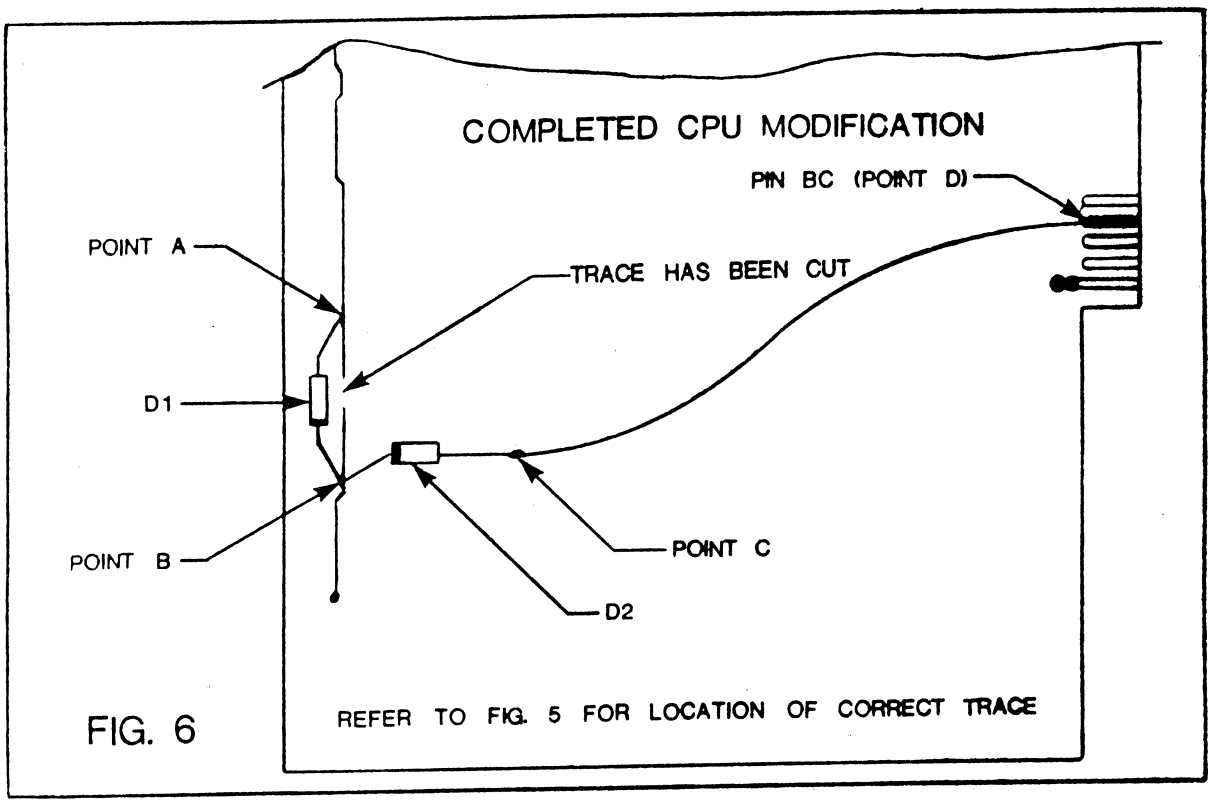

COMPLETED CPU MODIFICATION
PIN BC (POINT D)
POINT A
TRACE HAS BEEN CUT
D1
POINT B
POINT C
D2
REFER TO FIG. 5 FOR LOCATION OF CORRECT TRACE

FIG. 6

JUMPERS FROM CONTROLLER CARD CONNECTOR TO CPU BUS CONNECTOR

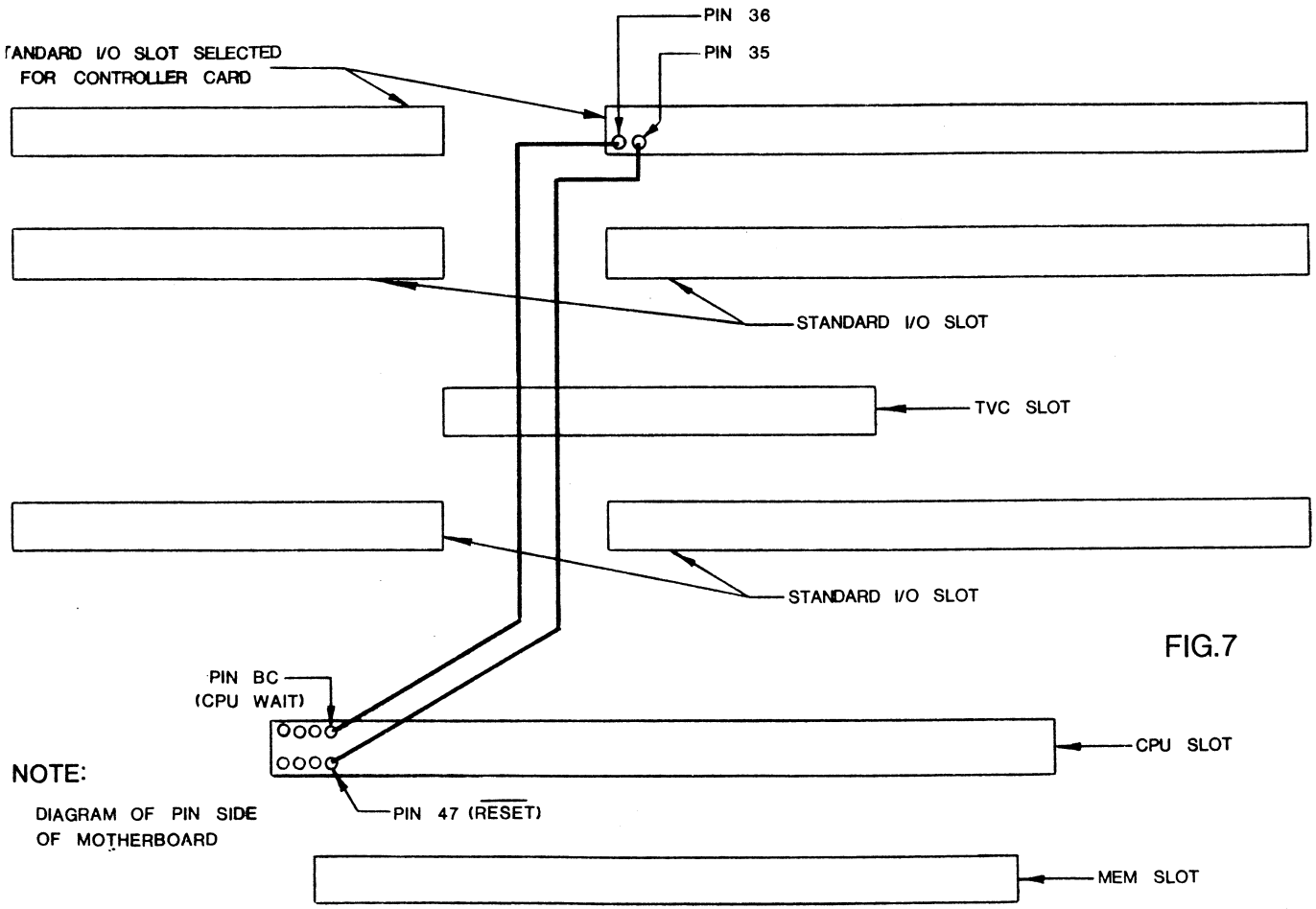


FIG.7

Software

DESCRIPTION

The software tape and listing provided give the user basic driver commands needed for operation. A comprehensive disk operating system will be available to integrate the driver routines into a user-oriented operating system.

The tape provided and the source listing at the end of this section give the user six basic commands.

READ— reads 128 bytes from the disk into the memory buffer location specified at address 014261 (low order address byte) and 014262 (high order address byte). The label for the data word is BUFFR. The parameter at this location on the tape is 014 (H) 312 (L), meaning data will be written into sequential memory locations beginning at address 014 (H) 312(L).

WRITE—writes 128 bytes from the memory location specified by BUFFR or on the tape specified as 0124 (H) 312 (L).

SEEK—moves the head on the drive to the track number specified by track.

INITIALIZE—moves the head to track 00 on the specified drive and unloads the head.

FORMAT—writes ID address marks at the beginning of all sectors on the disk.

RESTORE—zeros all the parameters and flags in the program and resets the head to track 0 on all drives.

Operating Instruction for Using the Tape

All parameters must be set before using or making a call to the program on the tape.

The parameters have initially been set to the following values.

COMMANDS

Octal	Description
001	READ
002	WRITE
003	SEEK
004	INITIALIZE
005	FORMAT
006	RESTORE

Location	Name	Description
014264	UNIT	Drive number in use (001-004), specified 001
014265	TRACK	Track address (001-116), specified 001
014266	SECTOR	Sector desired (003-035), specified 003
014267	SCTSZ	Number of bytes in block (003-200) specified 200
014261	BUFFR	Low order of data buffer,specified 312
014262		High order of data buffer, specified 014

Option 7 on the operations monitor display is the disk driver option and is vectored for execution beginning at page 6 address 000 or what is normally the beginning of the keyboard programmer address region.

The short program at page 6 carries out the following steps.

		Octal
Step 1	LOAD A with 04	076 004
Step 2	STORE A at 014 263	062 263 014
Step 3	CALL subroutine at 010 175	315 175 010
Step 4	LOAD A with 05	076 005
Step 5	STORE A at 014 263	062 263 014
Step 6	CALL subroutine at 010 175	315 175 010
Step 7	RESTART 7 (other jumps may be used)	377

The program as supplied executes an INITIALIZE command followed by a FORMAT command. During execution of the program the head will start at the outside track (track 00) and move toward the center of the disk, formatting each track and sector as it goes. If no problems have occurred in formatting and the head reaches the disk center, the program should return control to the operations monitor (or Options List).

All diskettes purchased from the Digital Group are unformatted and must be formatted before any other operations such as READ and WRITE can occur. Once the disk is formatted, any sequence of commands may be carried out in a manner similar to the sample program which formats the disk.

OPERATING PROCEDURE FOR TESTING THE DISK SYSTEM

At this point you should have finished with the assembly of the controller card, and the hook-up of the power supplies to the drives, and other cabling as documented earlier. You should also have made the CPU cabinet interconnection (if you have a Digital Group cabinet). It is important to verify all voltage connections as incorrect wiring may jeopardize your drives, controller card, and perhaps your system. Before connecting the +24V and +5V supply, verify the voltages both on the supply and on the corresponding Molex pins to be connected to the drive connector. Measure with reference to ground on the power supply.

Be sure, first of all, that your system is operating correctly, i.e., check voltages on the bus, run a memory test routine, and check to see that audio tapes are loading properly and that programs loaded from audio run correctly. A good software test is to load MAXI-BASIC. If MAXI-BASIC runs correctly, and the display comes up with MAXI-BASIC, READY, then there is a good chance that your system is running properly.

With power off to your system, install the drive cable assembly to the back of your CPU cabinet (or install appropriately if the drive connections are not made via a CPU cabinet). With the drive connector disconnected from the drive, verify all signal connections from the controller card slot (topside) to the drive connector. Also check the signal lines and voltage lines to see that none are shorted to ground or to other voltage lines. These tests may have been performed earlier as detailed in the previous assembly steps.

If all tests are correct, turn power on to your computer and verify the DC voltages on the controller card edge connector, and [illegible] connector.

NOTE: At the CPU cabinet, the drive cable assembly is installed according to the orientation as marked on the card.

The pins to check for Shugart Drives are:

1. Controller card 22-pin edge connector
   - pin 1, +5V
   - pin 22, +12V
   - pin A, +5V
   - pin B, -5V
   - pin Z, -12V

2. Drive edge connector, J5 (with drive supply connected)
   - pin 1, +24V DC
   - pin 5, +5V DC
   - **NOTE:** AC power to the drive is not connected, and the controller card is not installed. -5V is supplied through the controller card and will not appear at the drive unless the controller card is installed.

The pins to check for Innovex are:

1. Controller card 22-pin edge connector
   - pin 1, +5V
   - pin 22, +12V
   - pin A, +5V
   - pin B, -5V
   - pin Z, -12V

2. Drive paddlecard edge connector (with drive supply connected)
   - pins L2 & R2, +24V DC
   - pins L11 and R11, +5V DC
   - **NOTE:**AC power to the drive is not connected, and the controller card is not installed. -5V is supplied through the controller card and will not appear at the drive unless the controller card is installed.

3. Install the controller card (with all IC's mounted on the card). Verify that -5V is present both at pin 20 and pin X on the controller card pinout and at the power pins on the drive connector.

If all tests check out at this point, turn power off to the system and drive power supplies.

Install the AC connector to each drive in your system.

Turn power on to the drive power supplies and to the Digital Group computer. For convenience a switched outlet on the back of the CPU cabinet should by used for the drives' AC supply voltage.

With AC power on to the drive and the cable connected to the drive, further tests are made with the software driver routines (similar to the Phideck routines).

AC power applied to the drives runs the 360 rpm drive motor.

Do not disconnect AC or DC power to the drives or to the computer with diskettes inserted as damage may occur to the diskette.

SOFTWARE TESTING

The drive manual(s) included with Shugart drives provides both general and technical information about the drive. Included are user options, electrical and mechanical specifications of the disk drive, and the loading procedure for inserting diskettes. The drive manual(s) also includes a functional description of the drive with a discussion of interface requirements and signals. Finally, the manual includes information about maintenance, electrical pinouts on the drive connector, and sectional drawings of mechanical as well as electrical components.

Turn power on to the system with all integral components connected. If you have Innovex Drives remove or back out screws holding the hinged drive plate. Movements of the drive motor, the head stepping motor, and the head load mechanism can be observed with this top plate in an "up" position. Load in the audio tape supplied (disk driver routines). After loading the tape the screen should display the Option List with Option 7 being the disk driver execution option.

By selecting Option 7, the head will load, go to track 00 (outside track) if not there already, and travel in short increments to the inside track. Upon reaching the inside track, the Option List will return to the screen, or an error message will be displayed. Error messages are referenced on the last page of the source listing.

Errors might be indicated if signals are not sent from the controller card (i.e., HEAD LOAD, READ DATA, WRITE DATA pulses not present) or if signals are not properly connected to the drive or to the controller card. An oscilloscope is needed in many cases to test whether signals are actually present. Most problems will occur because of bad or incorrect connections, not because of card or drive failures. Problems can also occur if the diskette has not been inserted properly, or if the front door is not closed.

If the Option List reappears on the screen, the disk has been formatted on all tracks. The user may now modify the commands to test other operations such as READ and WRITE.

To properly test reading and writing, the data in the memory buffer at address 014 (H) 312 (L) should be filled with test patterns that will indicate whether a READ or WRITE operation has actually modified the buffer contents.

By using Options 3 or 4 (octal or hex keyboard programmer and storage dump) and addressing the memory buffer (H keyed, L keyed) the user can first modify the contents of whatever is in the buffer to a constant (such as 123). Be sure that the cursor (address pointer or arrow) is in the memory buffer and not outside it. The memory buffer starts at 014 (H) 312 (L) and runs to 015 (H) 011 (L).

To modify the program to write on the diskette, change the second byte 005 to 002 in step 4. To read from the disk, change the second byte to 001. Data in the memory buffer (an appropriate test pattern) should first be written onto the disk and then erased using the keyboard programmer. With the execution of a READ operation from the disk, the test pattern will be reloaded into the memory buffer.

A source listing is provided which gives the user routines for controlling the disk, i.e., reading, writing, initializing and formatting the diskettes. The NEC uPD372D controller chip manual is provided to give information about the controller chip pinout, interfacing requirements and the internal register structure of the chip. A section labeled Data Conditioner and Data Conditioner Algorithm provides information on transmitting data to and from the disk, and timing and data patterns such as ID address, data address, and deleted address marks used in IBM format and recognized by the controller chip. A last section is included describing routines such as reading ID marks, reading data, writing data, and start up and transfer control routines.

Controller Parts List

Label	Description	Qty.	Digital Group Part #
☐	Controller printed circuit board	1	090-046
☐ IC4	NEC uPD372 floppy controller chip, 42-pin	1	073-018
☐ IC1, IC10, IC26	7408 TTL IC, 14-pin	3	075-007
☐ IC3, IC11	74123 TTL IC, 16-pin	2	075-029
☐ IC6	9602 TTL IC, 16-pin	1	075-057
☐ IC8, IC12, IC14, IC15, IC16, IC18, IC20	7474 TTL IC, 14-pin	7	075-019
☐ IC9	75452 TTL IC, 8-pin	1	075-058
☐ IC13, IC24	7432 TTL IC, 14-pin	2	075-013
☐ IC19	7402 TTL IC, 14-pin	1	075-002
☐ IC21, IC30, IC33	7404 TTL IC, 14-pin	3	075-004
☐ IC29	74175 TTL IC, 16-pin	1	075-040
☐ IC32	7430 TTL IC, 14-pin	1	075-012
☐ IC22, IC25, IC28, IC31	N8T97B TTL IC, 16-pin	4	075-052
☐ IC34	74125 TTL IC, 14-pin	1	075-031
☐ IC2	7414 TTL IC, 14-pin	1	075-059
☐ IC5, IC7	7416 TTL IC, 14-pin	2	075-060
☐ IC17	8224 clock driver IC, 16-pin	1	073-000
☐ IC27	7410 TTL IC, 14-pin	1	075-009
☐ R1, R2, R17	47 ohm, ¼ watt resistor	3	001-006
☐ R11	220 ohm, ¼ watt resistor	1	001-013
☐ R9, R12, R14	5.1K ohm, ¼ watt resistor	3	001-033
☐ R10	8.2K ohm, ¼ watt resistor	1	001-036
☐ R8	10K ohm, ¼ watt resistor	1	001-037
☐ R15	20K ohm, ¼ watt resistor	1	001-047
☐ R16	22K ohm, ¼ watt resistor	1	001-040
☐ R13	100 ohm, ½ watt resistor	1	002-004
☐ R3, R4, R5, R6, R7	150 ohm, ½ watt resistor	5	002-008
☐ C1, C2, C4, C6, C10 - C14, C17 - C20, C22, C24, C26 - C30, C32 - C39, C41	.01 mfd ceramic disk, 25V	29	014-006
☐ C21	10 pf silver mica	1	018-001
☐ C15	82 pf silver mica	1	018-009

☐ C5	100 pfd, silver mica	1	018-003
☐ C3	200 pfd, silver mica	1	018-010
☐ C9	220 pfd, silver mica	1	018-004
☐ C8	750 pfd, silver mica	1	018-011
☐ C7	1000 pfd, silver mica	1	018-000
☐ C25, C31, C40	4.7 mfd, 35V tantalum	3	010-002
☐ C23	22 mfd, 15V tantalum	1	010-004
☐ C16	100 mfd, 25V electrolytic	1	012-008
☐ D1	1N3064 diode	1	040-002
☐ Y1	18MHz crystal	1	030-006
☐	8-pin socket	1	060-000
☐	14-pin socket	22	060-001
☐	16-pin socket	9	060-002
☐	42-pin socket	1	060-008
☐	Crystal socket	1	060-007
☐	36-pin wirewrap connector	1	080-001
☐	22-pin wirewrap connector	1	080-000
☐	Floppy Disk Controller Card documentation, including software tape and disk	1	298-078

CPU Modification Kit

☐ D1, D2	1N 4148 diode	2	040-006
☐	Utility wire—insulated 24-30 gauge	2'	560-003

```
FILE  060000  247062
READY
ASSM

247063                  0100 *SOFTWARE REV #28 10 AUG. '77; AUTHOR, G.L. PETERSON
247063                  0110 *THIS FDOS FOR REV.3 CONTROLLER PROTOTYPE BOARD
247063                  0120 *THIS IS A FLOPPY DISC CONTROLLER PROGRAM
247063                  0130 *BASED ON PUBLISHED DATA FOR THE NEC UPD372 CHIP
247063                  0140 *
247063                  0150 * CHIP DATA EQUATES
247063                  0160 WORST  EQU  80H RESET
247063                  0170 WOMBL  EQU  40H MUST BE LOW
247063                  0180 WOHLD  EQU  08H HEAD LOAD
247063                  0190 WOLCT  EQU  04H LOW CURRENT
247063                  0200 WOWFR  EQU  02H WRITE FAULT RESET
247063                  0210 W1CBS  EQU  80H CLOCK BIT STROBE
247063                  0220 W1CBN  EQU  38H CLOCK BITS FOR NORMAL DATA
247063                  0230 W1CBI  EQU  10H CLOCK BITS FOR INDEX ADDRESS MARK
247063                  0240 W1CBD  EQU  00H CLOCK BITS FOR ID,DATA,OR DELETED DATA
247063                  0250 W1UAS  EQU  04H UNIT A STROBE
247063                  0260 W1UAA  EQU  03H UNIT A ADDRESS MASK
247063                  0270 W3RCS  EQU  80H READ CLOCK SET
247063                  0280 W3WCS  EQU  40H WRITE CLOCK SET
247063                  0290 W3STT  EQU  20H START READ OR WRITE OPERATION
247063                  0300 W3WES  EQU  10H WRITE ENABLE SET
247063                  0310 W3IXS  EQU  08H INDEX START
247063                  0320 W3WER  EQU  04H WRITE ENABLE RESET
247063                  0330 W3CCG  EQU  02H CYCLIC CHECK GENERATE
247063                  0340 W3CCW  EQU  01H CYCLIC CHECK WORDS
247063                  0350 W4STS  EQU  80H STEP STROBE
247063                  0360 W4SID  EQU  40H STEP IN OR DIRECTION
247063                  0370 W4SOS  EQU  20H STEP OUT OR STEP
247063                  0380 W4SNS  EQU  0DFH THIS IS W4SOS BAR
247063                  0390 W4UBS  EQU  04H UNIT B STROBE
247063                  0400 W4UBA  EQU  03H UNIT B ADDRESS MASK
247063                  0410 W6TRR  EQU  04H TIMER REQUEST RESET
247063                  0420 W6IRR  EQU  02H INDEX REQUEST RESET
247063                  0430 W6DRR  EQU  01H DATA REQUEST RESET
247063                  0440 ROALH  EQU  80H ALWAYS HIGH UNDER NORMAL POWER CONDITIONS
247063                  0450 RORYB  EQU  40H READY B
247063                  0460 ROUBA  EQU  30H UNIT B ADDRESS MASK
247063                  0470 ROERR  EQU  08H WRITE FAULT ORDRIVE A READY OR COMMAND
247063                  0480 *OVERRUN ERROR; MUST BE CORRECTED BEFORE COMMANDING DRIVE
247063                  0490 ROTRQ  EQU  04H TIMER REQUEST
247063                  0500 ROIRQ  EQU  02H INDEX REQUEST
247063                  0510 RODRQ  EQU  01H DATA REQUEST
247063                  0520 R1WRT  EQU  80H WRITE MODE
247063                  0530 R1T00  EQU  40H TRACK 00
247063                  0540 R1DER  EQU  20H DATA ERROR (CRC TYPE )
```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```
247063                  0550 R1COR  EQU  10H COMMAND OVERRUN
247063                  0560 R1RYA  EQU  08H READY ON DRIVE A
247063                  0570 R1WFT  EQU  04H WRITE FAULT
247063                  0580 R1UAA  EQU  03H UNIT A ADDRESS MASK
247063                  0590 * SYSTEM PARAMETERS
247063                  0600 NU     EQU  01D NUMBER OF FLOPPY DISC DRIVES
247063                  0610 NTRKS  EQU  77D NUMBER OF TRACKS ON A DISC
247063                  0620 NSCTR  EQU  26D NUMBER OF SECTORS ON A DISC
247063                  0630 NBSCT  EQU  128D NUMBER OF DATA BYTES IN A SECTOR
247063                  0640 NTRYS  EQU  03H NUMBER OF READ RETRYS
247063                  0650 LHCTK  EQU  43D LAST HI CURRENT TRACK
247063                  0660 RVLIM  EQU  04H REVOLUTIN LIMIT IN IDLE LOOP WITH HD LDED
247063                  0670 STACK  EQU  002000 PUT THE STACK HERE
247063                  0680 *
247063                  0690 * I/O ASSIGNMENTS
247063                  0700 IOBAS  EQU  0F0H THIS IS THE START OF THE PORT ARRAY
247063                  0710 W0     EQU  IOBAS+0
247063                  0720 W1     EQU  IOBAS+1
247063                  0730 W2     EQU  IOBAS+2
247063                  0740 W3     EQU  IOBAS+3
247063                  0750 W4     EQU  IOBAS+4
247063                  0760 W6     EQU  IOBAS+6
247063                  0770 W7     EQU  IOBAS+7
247063                  0780 DATA   EQU  W2
247063                  0790 WAIT   EQU  W7
247063                  0800 HALT   EQU  W7
247063                  0810 R0     EQU  IOBAS+0
247063                  0820 R1     EQU  IOBAS+1
247063                  0830 R2     EQU  IOBAS+2
247063                  0840 *
247063                  0850 ********************************************************
010000                  0860        ST   0800H PUT ALL THIS ABOVE THE SUDING OP SYSTEM
010000                  0870 ********************************************************
010000                  0880 * INCOMING BRANCH TABLE
010000 303 076 010       0890        JP   INIT INITIALIZE DISC DRIVES AND SOFTWARE
010003 303 206 012       0900        JP   SEEK SEEK TO A TRACK AND SECTOR
010006 303 156 011       0910        JP   READ READ A SECTOR FROM A TRACK
010011 303 374 011       0920        JP   WRITE WRITE A SECTOR TO A TRACK
010014 303 161 013       0930        JP   FRMAT PUT AN IBM FORMAT ON A VIRGIN DISC
010017                  0940 *
010017                  0950 * OUTGOING BRANCH TABLE
010017 303 000 005       0960 VMON   JP   0500H VIDEO MONITOR RETURN
010022                  0970 *XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
010022                  0980 *INITIALIZE, COMMAND RETURN AND IDLE LOOP
010022 363               0990 RST0   DI    NO INTERRUPTS
010023 355 106           1000        IM   00 SET 8080 INTERRUPT MODE
010025 076 200           1010        LD   A,<WORST
010027 323 360           1020        OUT  <W0
010031 061 000 002       1030        LD   SP,STACK
```

```
010034                    1040 *INITIALIZE DATA AREA TO ZERO
010034 041 263 014        1050 RS020  LD   HL,CMND HL POINTS TO THE DATA AREA
010037 006 027            1060        LD   B,NB NUMBER OF BYTES IN THE DATA AREA
010041 257                1070        XOR  A 00 TO THE ACC
010042 167                1080 RS030  LD   M,A WRITE A 00
010043 043                1090        INC  HL
010044 005                1100        DEC  B LOOP COUNT
010045 040 373            1110        JR   NZ,RS030 LOOP WRITING ZEROS TO DATA AREA
010047                    1120 * INITIALIZE THE SECTOR SIZE
010047 076 200            1130        LD   A,NBSCT NUMBER OF BYTES IN A SECTOR TO ACC
010051 062 267 014        1140        LD   (SCTSZ),A
010054                    1150 * INITIALIZE ALL DISC UNITS
010054 076 001            1160        LD   A,01H START WITH DRIVE 1
010056 062 264 014        1170 RS010  LD   (UNIT),A SET UNIT # IN PARAMETER AREA
010061 315 076 010        1180        CALL INIT 00 TO WR0,UNLOAD THE HEAD, MOVE HEAD TO
010064                    1190 *TRACK 00, AND SET UP THE TRACK POINTER "TKPTR"
010064 072 264 014        1200        LD   A,(UNIT) LOAD UNIT # JUST INITIALIZED
010067 376 001            1210        CP   NU LAST UNIT?
010071 050 072            1220        JR   Z,RT010 IF DONE EXIT
010073 074                1230        INC  A NEXT DRIVE #
010074 030 360            1240        JR   RS010 GO DO NEXT UNIT
010076                    1250 *-------------------------------------------------------
010076                    1260 * INITIALIZE DISC UNIT SUBROUTINE
010076                    1270 *00 TO WR0, UNLOAD THE HEAD,GO TO TRACK 00, SET TKPTR
010076                    1280 INIT   EQU  $
010076 021 306 014        1290        LD   DE,WR0 BASE ADDRESS OF STORAGE LOCATIONS
010101 315 150 013        1300        CALL INDXA INDEXED ADDRESSING ROUTINE DE+(UNIT-1)
010104                    1310 * GOES TO HL
010104 257                1320        XOR  A 00 TO A
010105 167                1330        LD   M,A SET WR0 THIS DRIVE TO 00
010106 315 376 012        1340        CALL UNLD UNLOAD THE HEAD
010111                    1350 * MOVE HEAD TO TRACK 00
010111 016 114            1360        LD   C,NTRKS-1 LOOP LIMIT FOR TRACK SEEKING
010113                    1370 * EQUALS NUMBER OF TRACKS-1
010113 333 361            1380 IN010  IN   R1 READ STATUS OF THIS DRIVE
010115 057                1390        CPL
010116 346 100            1400        AND  R1T00 ARE WE ON TRACK 00?
010120 040 006            1410        JR   NZ,IN020 IF YES WE ARE DONE SO EXIT
010122 315 255 012        1420        CALL STO IF NOT CALL ROUTINE TO STEP OUT ONE TRACK
010125 015                1430        DEC  C DROP THE LOOP COUNT
010126 040 363            1440        JR   NZ,IN010 IF STILL IN THE LOOP STEP OUT AGAIN
010130                    1450 IN020  EQU  $
010130 021 307 014        1460        LD   DE,TKPTR THIS IS TRACK POINTER, THIS DRIVE
010133 315 150 013        1470        CALL INDXA
010136 257                1480        XOR  A 00 TO ACC
010137 167                1490        LD   M,A MAKE THIS TRACK 00 TO INITIALIZE SOFTWARE
010140 041 312 014        1500        LD   HL,BUF SET UP THE NORMAL BUFFER AREA
010143 042 261 014        1510        LD   (BUFFR),HL
010146 311                1520        RET  WE ARE DONE
```

```
010147                  1530 *-------------------------------------------------------
010147                  1540 *RETURN FROM A COMMAND TO THIS POINT
010147 363              1550 RETRN  DI    OUR UNDIVIDED ATTENTION
010150 050 013          1560        JR    Z,RT010 WAS THERE AN ERROR ON THE OPERATION?
010152 076 001          1570        LD    A,01H YES! LOAD 01 CODE
010154 062 270 014      1580        LD    (MERF),A AND SET THE MASTER ERROR FLAG
010157 315 376 012      1590        CALL  UNLD
010162 303 315 010      1600        JP    ERROR
010165 315 376 012      1610 RT010  CALL  UNLD
010170 076 000          1620        LD    A,00H
010172 062 263 014      1630        LD    (CMND),A
010175 072 263 014      1640 IDL10  LD    A,(CMND)
010200 267              1650        OR    A
010201 040 003          1660        JR    NZ,EXEC
010203 303 000 005      1670        JP    0500H
010206                  1680 *******************************************************
010206                  1690 * COMMAND EXECUTION
010206                  1700 * A=COMMAND
010206 117              1710 EXEC   LD    C,A SAVE THE COMMAND IN C
010207                  1720 * ZERO OUT THE FLAGS
010207 021 270 014      1730        LD    DE,MERF MASTER ERROR FLAG
010212 006 015          1740        LD    B,NF NUMBER OF FLAGS
010214 257              1750        XOR   A
010215 022              1760 EX005  LD    (DE),A WRITE A ZERO TO ALL ERROR FLAGS FROM
010216                  1770 * MERF ON DOWN FOR THE COUNT IN B
010216 023              1780        INC   DE
010217 005              1790        DEC   B
010220 040 373          1800        JR    NZ,EX005
010222 076 006          1810        LD    A,<NCMDS LIMIT OF VALID COMMANDS
010224 271              1820        CP    C COMMAND<MAX NUMBER OF VALID COMMANDS?
010225 362 235 010      1830        JP    P,EX010 YES
010230 062 271 014      1840        LD    (CMDER),A NO, SET COMMAND ERROR FLAG
010233 030 060          1850        JR    ERROR
010235                  1860 * CHECK ALL PARAMETERS FOR THE EXECUTION OF THIS COMMAND
010235 021 264 014      1870 EX010  LD    DE,UNIT DE=ADDRESS OF UNIT, FIRST PARAMETER
010240 041 235 014      1880        LD    HL,LMTBL HL=ADDRESS OF THE LIMIT TABLE
010243 006 004          1890        LD    B,NP B=NUMBER OF PARAMETERS
010245 032              1900 EX020  LD    A,(DE) A=PARAMETER TO BE CHECKED
010246 276              1910        CP    M LOWER LIMIT OK?
010247 332 310 010      1920        JP    C,EX040 NO, AN ERROR
010252 043              1930        INC   HL YES
010253 276              1940        CP    M UPPER LIMIT OK?
010254 322 310 010      1950        JP    NC,EX040 NO, AN ERROR
010257 043              1960        INC   HL YES, NEXT PARAMETER LOWER LIMIT IN TABLE
010260 023              1970        INC   DE NEXT PARAMETER
010261 005              1980        DEC   B LOOP DONE?
010262 040 361          1990        JR    NZ,EX020 NO
010264                  2000 *COMMAND AND PARAMETERS OK
010264 171              2010        LD    A,C RETRIEVE THE COMMAND
```

```
010265 041 245 014      2020        LD   HL,CTBL
010270 075              2030        DEC  A A=(0-(N-1))
010271 313 047          2040        SLA  A A=2*A
010273 137              2050        LD   E,A
010274 026 000          2060        LD   D,00H
010276 031              2070        ADD  HL,DE HL=ADDRESS OF ENTRY IN COMMAND TABLE
010277 136              2080        LD   E,M
010300 043              2090        INC  HL
010301 126              2100        LD   D,M DE=ADDRESS OF COMMAND SERVICE ROUTINE
010302 353              2110        EX   DE,HL IN HL NOW
010303 021 147 010      2120        LD   DE,RETRN THIS IS THE POINT TO RETURN TO
010306 325              2130        PUSH DE SET UP RETURN ADDRESS
010307 351              2140        JP   (HL) JUMP TO SERVICE ROUTINE
010310                  2150 *PARAMETER ERROR SERVICE SUBROUTINE
010310 076 001          2160 EX040  LD   A,01H ERROR CODE
010312 062 272 014      2170        LD   (PRMER),A SET THE PARAMETER ERROR FLAG
010315 062 270 014      2180 ERROR  LD   (MERF),A SET MASTER ERROR FLAG
010320 061 000 002      2190        LD   SP,STACK RESET THE STACK POINTER
010323 315 346 000      2200        CALL 00E6H SCREEN ERASE
010326 041 270 014      2210        LD   HL,MERF
010331 006 015          2220        LD   B,NF
010333 136              2230 ERRLP  LD   E,M
010334 315 041 002      2240        CALL 002041 HEX CHAR
010337 076 254          2250        LD   A,0ACH
010341 315 372 000      2260        CALL 000372
010344 043              2270        INC  HL
010345 005              2280        DEC  B
010346 040 363          2290        JR   NZ,ERRLP
010350 315 250 001      2300 ERLP1  CALL 01A8H KEYBOARD
010353 376 240          2310        CP   0A0H
010355 040 371          2320        JR   NZ,ERLP1
010357 303 000 005      2330        JP   0500H
010362                  2340 ************************************************************
010362                  2350 *READ ID RECORD ROUTINE
010362 315 206 012      2360 RID    CALL SEEK POSITION THE HEAD TO TRACK # IN "TRACK"
010365 315 332 012      2370        CALL HDLD LOAD THE HEAD
010370 016 004          2380        LD   C,04H THIS IS THE LIMIT OF REVOLUTIONS
010372                  2390 *PERMITTED WITHOUT FINDING CORRECT ID RECORD. 4 ASSURES
010372                  2400 *THREE COMPLETE REVOLUTIONS OF THE DISC
010372 041 265 014      2410 RIA    LD   HL,TRACK INITIALIZE TRACK/SECTR POINTER IN HL
010375 021 275 014      2420        LD   DE,WTRK INITIALIZE FLAG POINTER IN DE
011000 257              2430        XOR  A
011001 107              2440        LD   B,A B=A=00
011002 323 363          2450        OUT  <W3 RESET STT FOR RETRY
011004 076 240          2460        LD   A,W3RCS+W3STT READ CLOCK AND START BITS OF W3
011006 323 363          2470        OUT  <W3 GO TO READ CLOCK, SET STT AUTOMATICALLY
011010                  2480 *START READ OPERATION WHEN ADDRESS MARK IS READ
011010 323 367          2490        OUT  WAIT
011012                  2500 *WAITING FOR ADDRESS MARK
```

```
011012 333 362          2510        IN   <R2 READ THE DATA
011014 057              2520        CPL
011015 356 376          2530        XOR  OFEH IS IT AN ID ADDRESS MARK?
011017 040 105          2540        JR   NZ,RIM IF NOT JUMP TO ERROR SUBROUTINE
011021 323 367          2550        OUT  WAIT
011023                  2560 *WAITING FOR TRACK ADDRESS
011023                  2570 *WAITING FOR TRACK ADDRESS
011023 333 362          2580        IN   <R2 READ THE TRACK NUMBER
011025 057              2590        CPL
011026 256              2600        XOR  M COMPARE WITH DESIRED TRACK
011027 022              2610        LD   (DE),A WTRK=00 FOR OK
011030 023              2620        INC  DE DE POINTS TO ZERO1 BYTE
011031 323 367          2630        OUT  WAIT
011033                  2640 *WAITING FOR FIRST ZERO BYTE
011033 333 362          2650        IN   <R2 READ THE ZERO BYTE
011035 057              2660        CPL
011036 022              2670        LD   (DE),A ZERO1=00FOR OK
011037 023              2680        INC  DE DE POINTS TO ZERO2
011040 043              2690        INC  HL HL POINTS TO SECTR
011041 323 367          2700        OUT  WAIT
011043                  2710 *WAITING FOR SECTOR ADDRESS
011043 333 362          2720        IN   <R2 READ SECTOR ADDRESS BYTE
011045 057              2730        CPL
011046 256              2740        XOR  M COMPARE WITH DESIRED SECTOR
011047 107              2750        LD   B,A B=00 FOR OK
011050 076 041          2760        LD   A,W3STT+W3CCW
011052 323 363          2770        OUT  <W3 THIS COMMAND SENT TO W3 SETS CCW.(STT BIT
011054                  2780 *MUST ALSO BE SET TO AVOID RESETTING STT.) THE BIT RING
011054                  2790 *PULSE (BRP) FOLLOWING THE SETTING OF CCW WILL START A
011054                  2800 *BIT BY BIT COMPARISON OF THE DATA READ FROM THE DISC
011054                  2810 *WITH THE DATA READ FROM THE CRC REGISTER. THE CPU WILL
011054                  2820 *READ THE COMPLETED SECOND ZERO BYTE AT THE NEXT BRP,BUT
011054                  2830 *THE DRIVE HEAD WILL BEGIN READING THE FIRST CRC BYTE
011054 323 367          2840        OUT  WAIT
011056                  2850 *WAITING FOR SECOND ZERO BYTE
011056 333 362          2860        IN   <R2 READ SECOND ZERO BYTE
011060 057              2870        CPL
011061 022              2880        LD   (DE),A ZERO2=00 FOR OK
011062 023              2890        INC  DE
011063 323 367          2900        OUT  WAIT
011065                  2910 *WAITING FOR CRC BYTE #1
011065 076 040          2920        LD   A,W3STT TURN OFF CCW
011067 323 363          2930        OUT  <W3 STT=1; CCW=0; CCW IS RESET AT NEXT BRP
011071                  2940 *BIT-BY-BIT CRC COMPARISON WILL END
011071 323 367          2950        OUT  WAIT
011073                  2960 *WAITING FOR CRC BYTE #2
011073 333 361          2970        IN   R1 GET STATUS
011075 057              2980        CPL
011076 346 040          2990        AND  R1DER WAS THERE A CRC ERROR ON THE READ?
```

```
011100 022
011101 170
011102
011102 267
011103 040 021
011105
011105 323 367
011107
011107 353
011110 266
011111 053
011112 000
011113 053
011114 266
011115 323 367
011117
011117 053
011120 266
011121 040 003
011123 323 367
011125
011125 311
011126
011126
011126 333 360
011130 057
011131 346 002
011133 312 372 010
011136 323 366
011140 015
011141 302 372 010
011144 257
011145 323 363
011147 076 001
011151 062 274 014
011154 267
011155 311
011156
011156
011156
011156
011156 315 362 010
011161 300
011162 076 140
011164 323 363
011166 006 011
011170 323 367
011172
011172 005
```

```
3000        LD   (DE),A CRCID=00 FOR OK
3010        LD   A,B B HAS COMPARISON OF DESIRED SECTOR WITH
3020 *THE SECTOR READ
3030        OR   A SECTOR OK?
3040        JR   NZ,RIM ERROR HERE
3050 *PROPER SECTOR ID READ WITHOUT ERROR
3060        OUT  WAIT
3070 *WAITING FOR FIRST GAP BYTE
3080        EX   DE,HL HL POINTS TO CRCID, A=00
3090        OR   M TEST CRCID
3100        DEC  HL
3110        NOP   SHOULD BE OR,M TO TEST ZERO BYTE #2
3120        DEC  HL
3130        OR   M TEST ZERO1
3140        OUT  WAIT
3150 *WAITING FOR SECOND GAP BYTE
3160        DEC  HL
3170        OR   M TEST WTRK; TRACK ADDRESS=TRACK POINTER
3180        JR   NZ,RIM ERROR IF ANY BITS SET IN THE ABOVE
3190        OUT  WAIT
3200 *WAITING FOR THIRD GAP BYTE
3210        RET  NORMAL RETURN, ZERO FLAG=1
3220 *
3230 *ERROR PROCESSING ROUTINE FOR READ ID RECORD ROUTINE
3240 RIM    IN   <R0 READ STATUS
3250        CPL
3260        AND  R0IRQ WAS INTERRUPT AN INDEX REQUEST?
3270        JP   Z,RIA NO, WAIT FOR NEXT MARK
3280        OUT  <W6 YES, AN IRQ RESET TO W6
3290        DEC  C DECREMENT REVOLUTION LIMIT COUNTER
3300        JP   NZ,RIA WAIT FOR NEXT MARK IF NOT THIRD REV
3310        XOR  A THIRD REV WITHOUT SUCCESS SO QUIT
3320        OUT  <W3 RESET STT
3330        LD   A,01H ERROR CODE
3340        LD   (NOGO),A COULD NOT FIND REQUESTED ID
3350        OR   A CLEAR THE ZERO FLAG
3360        RET   AND TAKE THIS ERROR RETURN
3370 ********************************************************
3380 *READ DATA RECORD COMMAND ROUTINE
3390 *READ DATA RECORD ROUTINE
3400 *CALLS READ ID RECORD FIRST
3410 READ   CALL RID READ THE ID RECORD
3420        RET  NZ IF ERROR FOUND IN READ, RETURN
3430        LD   A,<W3WCS+<W3STT WRITE CLOCK SET AND START
3440        OUT  <W3 SET WRITE CLOCK, LEAVE STT SET
3450        LD   B,09H PASS GAP BYTES 4-12
3460 RGAP   OUT  WAIT
3470 *.WAITING FOR GAP BYTES 4 THROUGH 12
3480        DEC  B
```


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```
011173 040 373          3490        JR   NZ,RGAP
011175 323 367          3500        OUT  WAIT WAIT FOR GAP BYTE 13 HEAD PAST AREA
011177                  3510 *IN GAP THAT CONTAINS UNKNOWN INFORMATION GENERATRED WHEN
011177                  3520 *WRITE CURRENT WAS TURNED ON TO WRITE DATA RECORD.
011177                  3530 *
011177                  3540 *WAITING FOR GAP BYTE 13
011177 076 100          3550        LD   A,<W3WCS RESET STT, SET WRITE CLOCK, PREVENTS
011201 323 363          3560        OUT  <W3 INTERRUPTS UNTIL THE FOLLOWING IS DONE
011203 052 261 014      3570        LD   HL,(BUFFR) HL POINTS TO FIRST BYTE OF DATA
011206 026 041          3580        LD   D,W3STT+W3CCW COMMAND TO SET CCW IN D
011210 016 373          3590        LD   C,0FBH DATA ADDRESS MARK CODE TO C
011212 072 267 014      3600        LD   A,(SCTSZ) SET SECTOR SIZE IN ACC
011215 326 003          3610        SUB  03H
011217 107              3620        LD   B,A SAVE THE COUNT IN B
011220 076 240          3630        LD   A,W3RCS+W3STT SET READ CLOCK AND STT
011222 323 363          3640        OUT  <W3
011224 323 367          3650        OUT  WAIT
011226                  3660 *WAITING FOR ADDRESS MARK
011226 333 362          3670        IN   <R2
011230 057              3680        CPL
011231 271              3690        CP   C IS IT A DATA ADDRESS MARK?
011232 040 076          3700        JR   NZ,MARK IF NOT JUMP TO MARK
011234 323 367          3710        OUT  WAIT
011236                  3720 *WAITING FOR DATA BYTE #1
011236 333 362          3730        IN   <R2 IT WAS AN ADDRESS MARK, GET DATA BYTE 1
011240 057              3740        CPL
011241 167              3750        LD   M,A STORE FIRST DATA BYTE
011242 043              3760 RLOOP  INC  HL READ AND STORE DATA BYTES
011243 323 367          3770        OUT  WAIT
011245                  3780 *WAITING FOR DATA BYTES 2 THROUGH SECTOR SIZE-2
011245 333 362          3790        IN   <R2
011247 057              3800        CPL
011250 167              3810        LD   M,A
011251 005              3820        DEC  B
011252 302 242 011      3830        JP   NZ,RLOOP RELATIVE ADDRESSING TOO SLOW!
011255 043              3840        INC  HL
011256 323 367          3850        OUT  WAIT
011260                  3860 *WAITING FOR DATA BYTE # SECTOR SIZE-1
011260 333 362          3870        IN   <R2
011262 057              3880        CPL
011263 167              3890        LD   M,A
011264 172              3900        LD   A,D SET CCW TO ACCUMULATOR
011265 323 363          3910        OUT  <W3
011267 323 367          3920        OUT  WAIT
011271                  3930 *WAITING FOR DATA BYTE # SECTOR SIZE
011271 043              3940        INC  HL
011272 333 362          3950        IN   <R2
011274 057              3960        CPL
011275 167              3970        LD   M,A
```

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011276 323 367          3980        OUT  WAIT
011300                  3990 *WAITING FOR FIRST CRC BYTE
011300 076 040          4000        LD   A,W3STT
011302 323 363          4010        OUT  <W3 RESET CCW
011304 323 367          4020        OUT  WAIT
011306                  4030 *WAITING FOR THE SECOND CRC BYTE
011306 333 361          4040        IN   R1 READ THE STATUS
011310 057              4050        CPL
011311 107              4060        LD   B,A SAVE STATUS IN B
011312 257              4070        XOR  A 00 TO ACC
011313 323 363          4080        OUT  <W3 RESET STT. CHIP GOES TO WRITE CLOCK
011315 170              4090        LD   A,B RECALL STATUS
011316 346 040          4100        AND  R1DER IS THERE A CRC ERROR?
011320 062 301 014      4110        LD   (CRCDR),A SET CRC DATA RECORD FLAG
011323 050 003          4120        JR   Z,RD010 TAKE THIS EXIT IF ALL OK
011325 303 360 011      4130        JP   MK030 A CRC ERROR FOUND
011330 000              4140 RD010  NOP   LD (BUFFR),HL HERE SAVES UPDATED POINTER
011331 311              4150        RET
011332                  4160 *READ DATA RECORD ERROR SERVICE ROUTINE
011332 257              4170 MARK   XOR  A
011333 323 363          4180        OUT  <W3 RESET STT
011335 333 362          4190        IN   <R2 READ MARK AGAIN
011337 057              4200        CPL
011340 326 370          4210        SUB  0F8H IS IT A DELETED DATA MARK?
011342 062 302 014      4220        LD   (ILLMK),A SET ILLEGAL MARK FLAG
011345 302 354 011      4230        JP   NZ,MK010 ILLEGAL MARK
011350 074              4240        INC  A DELETED DATA MARK
011351 303 355 011      4250        JP   MK020
011354                  4260 *ILLEGAL MARK SERVICE ROUTINE
011354 257              4270 MK010  XOR  A ILLEGAL MARK
011355 062 303 014      4280 MK020  LD   (DELMK),A SET DELETED DATA MARK FLAG
011360 041 305 014      4290 MK030  LD   HL,RRTRY CHECK FOR A RETRY
011363 065              4300        DEC  M
011364 302 156 011      4310        JP   NZ,READ TRY AGAIN
011367 257              4320        XOR  A
011370 323 363          4330        OUT  <W3 RESET STT
011372 074              4340        INC  A CLEAR ZERO FLAG TO INDICATE ERROR CONDITION
011373 311              4350        RET
011374                  4360 ********************************************************
011374                  4370 *WRITE DATA RECORD COMMAND ROUTINE
011374                  4380 *PARAMETER AREA HAS THE #'S CONTROLLING THIS WRITE
011374 315 017 013      4390 WRITE  CALL FUR
011377 315 362 010      4400        CALL RID READ ID RECORD FIRST
012002 300              4410        RET  NZ EXIT IF ERROR IN ID RECORD READ
012003 006 011          4420        LD   B,09H WE WILL COUNT 9 INTERRUPTS FROM ID
012005 323 367          4430 WGAP   OUT  WAIT
012007                  4440 *WAITING FOR DRIVE TO BEGIN READING THE 10TH BYTE
012007 005              4450        DEC  B
012010 040 373          4460        JR   NZ,WGAP
```

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012012 076 270          4470        LD   A,W1CBS+W1CBN SET CLOCK BITS AND STROBE
012014 323 361          4480        OUT  <W1 SET THE WRITE CLOCK TO WRITE ALL POSSIBLE
012016                  4490 *CLOCK BITS (FF) FOR DATA
012016 257              4500        XOR  A
012017 323 362          4510        OUT  <W2 SET WRITE DATA REGISTER TM 00
012021 323 367          4520        OUT  WAIT
012023                  4530 *WAITING FMR 10TH INTERRUPT SINCE ID RECORD. HEAD IS
012023                  4540 *READING GAP BYTE 11
012023 076 160          4550        LD   A,<W3WCS+W3STT+<W3WES  WCS=STT=WES=1
012025 323 363          4560        OUT  <W3 WRITE CURRENT & WRITE CLOCK WILL START
012027                  4570 *AT NEXT BRP
012027 333 361          4580        IN   R1 READ STATUS
012031 057              4590        CPL
012032 346 004          4600        AND  R1WFT WRITE FAULT PRESENT?
012034 312 052 012      4610        JP   Z,WR010 IF NOT CONTINUE
012037 315 017 013      4620        CALL FUR RESET FILE UNSAFE
012042 076 001          4630        LD   A,01H
012044 062 304 014      4640        LD   (WRITF),A SET THE WRITE FAULT FLAG
012047 303 315 010      4650        JP   ERROR AND TAKE THE ERROR EXIT
012052 323 367          4660 WR010  OUT  WAIT
012054                  4670 *
012054 323 367          4680        OUT  WAIT HEAD BEGINS WRITING 00 IN GAP BYTE 12
012056                  4690 *
012056 323 367          4700        OUT  WAIT 12TH INTERRUPT; 00 TO BYTE 13
012060                  4710 *
012060 323 367          4720        OUT  WAIT 13TH INTERRUPT; 00 TO BYTE 14
012062                  4730 *
012062 052 261 014      4740        LD   HL,(BUFFR) SET HL TO START OF WRITE DATA
012065 323 367          4750        OUT  WAIT 14TH INTERRUPT 00 TO BYTE 15
012067                  4760 *
012067 006 373          4770        LD   B,0FBH LOAD A DATA MARK IN B
012071 323 367          4780        OUT  WAIT 15TH INTERRUPT; 00 TO BYTE 16
012073                  4790 *
012073 016 062          4800        LD   C,W3STT+W3CCG+W3WES SET CCG COMMAND TO C
012075 026 270          4810        LD   D,W1CBS+W1CBN STORE FF CLOCK PATTERN COMMAND
012077 036 060          4820        LD   E,W3STT+W3WES RESET CCG COMMAND TO E
012101 076 200          4830        LD   A,W1CBS+W1CBD STORE C7 DATA MARK CLOCK
012103                  4840 *PATTERN COMMAND IN A
012103 323 367          4850        OUT  WAIT
012105                  4860 *16TH INTERRUPT, HEAD IS WRITING 17TH AND LAST GAP BYTE
012105 323 361          4870        OUT  <W1 SET C7 DATA MARK CLOCK PATTERN. 16TH
012107 170              4880        LD   A,B SET FB DATA BITS FOR DATA MARK
012110 323 362          4890        OUT  <W2
012112 171              4900        LD   A,C SET CCG CAUSING CRC CALCULATION TO BEGIN
012113                  4910 *AT THE NEXT BRP
012113 323 363          4920        OUT  <W3
012115 172              4930        LD   A,D GET FF DATA BIT CLOCK PATTERN IN A
012116 323 367          4940        OUT  HALT
012120                  4950 *HEAD STARTS DATA MARK NEXT
```

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012120 323 361          4960        OUT  <W1 SET FF CLOCK, HEAD NOW BEGINS WRITING THE
012122                  4970 *DATA MARK
012122 173              4980        LD   A,E RESET CCG. CCG MUST BE RESET BEFORE NEXT
012123                  4990 *BRP OR CRC CALCULATION WOULD BEGIN AGAIN
012123 323 363          5000        OUT  <W3
012125 176              5010        LD   A,M LOAD IN FIRST DATA BYTE
012126 323 362          5020        OUT  <W2 WRITE BYTE #1
012130 323 367          5030        OUT  HALT
012132                  5040 *WAITING FOR CHIP TO FINISH DATA MARK AND START DATA
012132 072 267 014      5050        LD   A,(SCTSZ) SET THE SECTOR SIZE
012135 075              5060        DEC  A LESS THE BYTE JUST WRITTEN
012136 107              5070        LD   B,A THIS IS THE LOOP COUNT IN B
012137 043              5080 WLOOP  INC  HL WRITE DATA BYTES 2 THROUGH NBSCT
012140 176              5090        LD   A,M
012141 323 362          5100        OUT  <W2
012143 323 367          5110        OUT  HALT
012145                  5120 *HEAD WRITING DATA BYTES 2 THROUGH SCTSIZ
012145 005              5130        DEC  B
012146 302 137 012      5140        JP   NZ,WLOOP RELATIVE ADDRESSING TOO SLOW
012151 076 061          5150        LD   A,W3STT+W3CCW+W3WES SET CCW; IN WRITE MODE
012153                  5160 *CHIP WILL BEGIN WRITING BITS FROM THE CRC REGISTER AT
012153                  5170 *THE NEXT BRP FOLLOWING THE SETTING OF CCW. HEAD IS
012153                  5180 *WRITING DATA BYTE 128
012153                  5190 *WAITING FOR HEAD TO FINISH DATA
012153 323 363          5200        OUT  <W3
012155 323 367          5210        OUT  HALT
012157                  5220 *
012157 323 367          5230        OUT  HALT
012161                  5240 *
012161 076 377          5250        LD   A,OFFH LOAD FF GAP BYTE IN WRITE DATA REG.
012163 323 362          5260        OUT  <W2 HEAD BEGINS WRITING 2ND CRC BYTE
012165 076 060          5270        LD   A,W3STT+W3WES RESET CCW; WRITING
012167 323 363          5280        OUT  <W3 WILL STOP AT NEXT BRP
012171 323 367          5290        OUT  HALT
012173                  5300 *WAITING FOR HEAD TO FINISH 2ND CRC BYTE
012173 076 044          5310        LD   A,W3STT+W3WER WRITE ENABLE RESET. WRITE
012175                  5320 *CURRENT WILL STOP AT NEXT BRP. HEAD BEGINS WRITING FIRST
012175                  5330 *GAP BYTE
012175 323 363          5340        OUT  <W3 RESET CCW
012177 323 367          5350        OUT  HALT
012201                  5360 *WAITING FOR HEAD TO FINISH 1ST GAP BYTE
012201 257              5370        XOR  A RESET STT
012202 323 363          5380        OUT  <W3
012204 000              5390        NOP   LD (BUFFR),HL HERE SAVES UPDATED POINTER
012205 311              5400        RET  DATA RECORD HAS BEEN WRITTEN
012206                  5410 ****************************************************
012206                  5420 *GENERAL SUBROUTINES FOR CONTROL OF DRIVE
012206                  5430 *SEEK TRACK ROUTINE
012206                  5440 SEEK   EQU  $
```

```
012206 021 307 014      5450        LD   DE,TKPTR ADDRESS OF CURRENT DISC TRACK
012211 315 150 013      5460        CALL INDXA HL WILL EQUAL ADDRESS OF TRACK POINTER
012214 072 265 014      5470        LD   A,(TRACK) THIS IS THE TRACK DESIRED
012217 276              5480        CP   M
012220 050 015          5490        JR   Z,SKO20 EXIT IF WE ARE THERE
012222 372 232 012      5500        JP   M,SKO10 TKPTR>TRACK, SO STEP OUT
012225 315 243 012      5510        CALL STI TKPTR<TRACK, STEP IN
012230 030 354          5520        JR   SEEK
012232 315 255 012      5530 SKO10  CALL STO
012235 030 347          5540        JR   SEEK
012237 315 324 012      5550 SKO20  CALL STO40 AN ADDITIONAL 10 MS FOR HEAD SETTLING
012242 311              5560        RET
012243                  5570 *-------------------------------------------------------
012243                  5580 *STEP SUBROUTINES
012243                  5590 *STEP IN
012243 315 053 013      5600 STI    CALL UNSCL PREPARE TO COMMAND THE DRIVE
012246 006 340          5610        LD   B,W4STS+W4SID+W4SOS
012250 076 001          5620        LD   A,01H INCREMENT TKPTR
012252 303 264 012      5630        JP   STO10
012255                  5640 *STEP OUT
012255 315 053 013      5650 STO    CALL UNSCL MAKE THE DRIVE CURRENT
012260 006 240          5660        LD   B,W4STS+W4SOS STEP STROBE AND STEP OUT
012262 076 377          5670        LD   A,OFFH DECREMENT THE TRACK POINTER
012264                  5680 STO10  EQU  $
012264 021 307 014      5690        LD   DE,TKPTR
012267 315 150 013      5700        CALL INDXA INDEXED ADDRESSING
012272 206              5710        ADD  M INC/DEC TKPTR
012273 167              5720        LD   M,A RESTORE THE TKPTR
012274 072 053 000      5730        LD   A,(LHCTK) CHECK FOR WRITE CURRENT CHANGE
012277                  5740 *LHCTK=LAST HIGH CURRENT TRACK
012277 276              5750        CP   M A=LHCTK=TKPTR
012300 076 004          5760        LD   A,WOLCT LOW CURRENT BIT OF WO
012302 372 312 012      5770        JP   M,STO20 TRACK>LHCTK
012305 315 034 013      5780        CALL CLRWO TRACK<=LHCTK TURN OFF LOW CURRENT
012310 030 003          5790        JR   STO30
012312 315 043 013      5800 STO20  CALL SETWO TRACK>LHCTK SO SET THE BIT
012315 170              5810 STO30  LD   A,B STEP STROBE+STEP OUT
012316 323 364          5820        OUT  <W4 RISING EDGE OF SOS
012320 346 337          5830        AND  W4SNS W4SNS IS W4SOS BAR; TURN OFF SOS
012322 323 364          5840        OUT  <W4 TRAILING EDGE OF SOS
012324                  5850 *DELAY 10 MS FOR THE MOTOR TO RESPOND
012324 006 012          5860 STO40  LD   B,10D
012326 315 131 013      5870        CALL DELAY
012331 311              5880        RET
012332                  5890 *-------------------------------------------------------
012332                  5900 *HEAD LOAD SUBROUTINE
012332                  5910 HDLD   EQU  $ CHECK THE HEAD STATUS
012332 021 311 014      5920        LD   DE,HEAD BASE ADDRESS
012335 315 150 013      5930        CALL INDXA INDEXED ADDRESSING
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```
012340 176             5940        LD   A,M HEAD LOADED FLAG TO A; 1=LOADED
012341 267             5950        OR   A SET FLAGS; IS THE HEAD LOADED ALREADY?
012342 300             5960        RET  NZ IF SO RETURN
012343 315 053 013     5970        CALL UNSCL IF HEAD NOT LOADED SELECT THE DRIVE
012346 076 010         5980        LD   A,WOHLD
012350 315 043 013     5990        CALL SETWO LOAD THE HEAD
012353 006 036         6000        LD   B,30D WAIT 30 MS
012355 315 131 013     6010        CALL DELAY
012360 076 002         6020        LD   A,WOWFR
012362 315 043 013     6030        CALL SETWO
012365 076 002         6040        LD   A,WOWFR
012367 315 034 013     6050        CALL CLRWO
012372 076 001         6060        LD   A,01H SET THE HEAD STATUS
012374 030 011         6070        JR   ULO10
012376                 6080 *UNLOAD HEAD SUBROUTINE
012376 315 053 013     6090 UNLD   CALL UNSCL SET UP THE DRIVE
013001 076 010         6100        LD   A,WOHLD
013003 315 034 013     6110        CALL CLRWO UNLOAD THE HEAD
013006 257             6120        XOR  A
013007                 6130 ULO10  EQU  $
013007 021 311 014     6140        LD   DE,HEAD BASE ADDRESS
013012 315 150 013     6150        CALL INDXA
013015 167             6160        LD   M,A SET UP THE HEAD FLAG
013016 311             6170        RET
013017                 6180 *-------------------------------------------------------
013017                 6190 *FILE UNSAFE RESET ROUTINE
013017 076 002         6200 FUR    LD   A,02H
013021 345             6210        PUSH HL
013022 315 043 013     6220        CALL SETWO
013025 076 002         6230        LD   A,02H
013027 315 034 013     6240        CALL CLRWO
013032 341             6250        POP  HL
013033 311             6260        RET
013034                 6270 *-------------------------------------------------------
013034                 6280 *WRO MANAGER; MAINTAINS A SOFTWARE IMAGE OF WO
013034 041 306 014     6290 CLRWO  LD   HL,WRO
013037 057             6300        CPL
013040 246             6310        AND  M CLEAR
013041 030 004         6320        JR   CRO10
013043 041 306 014     6330 SETWO  LD   HL,WRO
013046 266             6340        OR   M SET
013047 323 360         6350 CRO10  OUT  <WO
013051 167             6360        LD   M,A SAVE A COPY OF WO
013052 311             6370        RET
013053                 6380 *-------------------------------------------------------
013053                 6390 *UNIT SELECT SUBROUTINE
013053 076 004         6400 UNSCL  LD   A,W1UAS SET THE SELECT STROBE
013055 323 361         6410        OUT  W1 DESELECT ALL "A" DRIVES
013057 323 364         6420        OUT  W4 DESELECT ALL "B" DRIVES
```

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013061 072 264 014      6430        LD   A,(UNIT) THIS IS THE DRIVE WE WANT
013064 376 003          6440        CP   03H DRIVES A OR B?
013066 362 116 013      6450        JP   P,UNO10 DRIVE 3 OR 4 IF NEGATIVE
013071 346 003          6460        AND  W1UAA MASK OUT THE UNIT NUMBER
013073 366 004          6470        OR   W1UAS TURN ON THE SELECT STROBE
013075 323 361          6480        OUT  W1 AND SELECT THE UNIT
013077 000              6490 UNOUT  NOP
013100 000              6500        NOP  GIVD THE DRIVE SOME TIME TO RESPOND
013101 333 361          6510        IN   R1 DRIVE STATUS
013103 057              6520        CPL
013104 346 010          6530        AND  R1RYA DRIVE READY?
013106 300              6540        RET  NZ YES
013107 057              6550        CPL   DRIVE NOT READY
013110 062 273 014      6560        LD   (SLCTF),A SET SELECT ERROR FLAG
013113 303 315 010      6570        JP   ERROR
013116 346 003          6580 UNO10  AND  W4UBA MASK OUT UNIT NUMBER
013120 326 002          6590        SUB  02H BIAS DOWN FOR DRIVE 3 OR 4
013122 366 004          6600        OR   W4UBS TURN ON THE SELECT STROBE
013124 323 364          6610        OUT  W4 SELECT THE UNIT
013126 303 077 013      6620        JP   UNOUT AND GO SEE IF IT COMES READY
013131                  6630 *-------------------------------------------------
013131                  6640 *DELAY SUBROUTINE
013131 076 004          6650 DELAY  LD   A,W6TRR TURN ON TIMER REQUEST
013133 323 366          6660        OUT  <W6 RESET TIMER REQUEST
013135                  6670 *WAIT FOR TRQ RST STATUS
013135 333 360          6680 D010   IN   <R0 READ STATUS
013137 057              6690        CPL
013140 346 004          6700        AND  <R0TRQ CHECK TRQ
013142 050 371          6710        JR   Z,D010 WAIT FOR A MS
013144 005              6720        DEC  B DONE?
013145 040 362          6730        JR   NZ,DELAY NO
013147 311              6740        RET  YES
013150                  6750 *-------------------------------------------------
013150                  6760 *INDEXED ADDRESSING SUBROUTINE
013150                  6770 *INPUT: DE=BASE; UNIT=INDEX. OUTPUT: HL=DE+(UNIT-1)
013150 041 264 014      6780 INDXA  LD   HL,UNIT DRIVE BEING COMMANDED
013153 156              6790        LD   L,M
013154 046 000          6800        LD   H,00H
013156 055              6810        DEC  L
013157 031              6820        ADD  HL,DE
013160 311              6830        RET
013161                  6840 *-------------------------------------------------
013161                  6850 *DISC FORMATTING COMMAND ROUTINE
013161 315 076 010      6860 FRMAT  CALL INIT HEAD TO TRACK 00
013164 315 332 012      6870        CALL HDLD LOAD THE HEAD
013167 041 001 000      6880        LD   HL,0001H H=00=TRACK ADDRESS; L=01=SECTOR
013172                  6890 *SET UP COMMANDS
013172 315 017 013      6900 FM030  CALL FUR
013175 076 270          6910        LD   A,<W1CBS+<W1CBN
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013177 323 361          6920        OUT  <W1 SET THE CLOCK BITS
013201 076 377          6930        LD   A,0FFH
013203 323 362          6940        OUT  <W2
013205 257              6950        XOR  A RESET STT
013206 323 363          6960        OUT  <W3
013210 076 170          6970        LD   A,<W3WCS+<W3STT+<W3WES+<W3IXS
013212 323 363          6980        OUT  <W3 SET CHIP TO START WRITING AT INDEX HOLE
013214 323 367          6990        OUT  HALT
013216                  7000 *INDEX START HEAD IS WRITING FIRST GAP BYTE
013216 076 002          7010        LD   A,<W6IRR
013220 323 366          7020        OUT  <W6 RESET INDEX REQUEST
013222                  7030 *WRITE PRE INDEX GAP
013222 006 047          7040        LD   B,39D B=# OF 0FFH GAP BYTES
013224 323 367          7050 FM040  OUT  HALT
013226                  7060 *
013226                  7070 *HEAD WRITES GAP BYTES 2 THROUGH 40
013226 005              7080        DEC  B DONE?
013227 040 373          7090        JR   NZ,FM040 IF NOT REPEAT
013231 257              7100        XOR  A YES, CHANGE GAP
013232 323 362          7110        OUT  <W2 BYTE TO 00H
013234 006 005          7120        LD   B,05H B=BYTE COUNT
013236 323 367          7130 FM050  OUT  HALT
013240                  7140 *
013240                  7150 *HEAD WRITES GAP BYTES 41 TROUGH 45
013240 005              7160        DEC  B DONE?
013241 040 373          7170        JR   NZ,FM050 NO, REPEAT
013243 323 367          7180        OUT  HALT
013245                  7190 *
013245                  7200 *HEAD IS WRITING GAP BYTE 46
013245                  7210 *WRITE INDEX ADDRESS MARK
013245 076 220          7220        LD   A,<W1CBS+<W1CBI
013247 323 361          7230        OUT  <W1 CHANGE CLOCK BITS TO D7
013251 076 374          7240        LD   A,0FCH
013253 323 362          7250        OUT  <W2 SET WRITE DATA=0FCH
013255 323 367          7260        OUT  HALT
013257                  7270 *
013257                  7280 *HEAD IS WRITING INDEX ADDRESS MARK
013257                  7290 *WRITE POST INDEX GAP
013257 076 270          7300        LD   A,<W1CBS+<W1CBN
013261 323 361          7310        OUT  <W1 SET CLOCK BITS TO FF
013263 076 377          7320        LD   A,0FFH
013265 323 362          7330        OUT  <W2 SET WRITE DATA TO 0FFH
013267 006 031          7340        LD   B,25D B=BYTE COUNT
013271 323 367          7350 FM060  OUT  HALT
013273                  7360 *
013273                  7370 *HEAD WRITES GAP BYTES 1 THROUGH 26
013273 005              7380        DEC  B DONE?
013274 040 373          7390        JR   NZ,FM060 NO, REPEAT
013276 257              7400 FM070  XOR  A BEGINNING OF SECTOR WRITE LOOP. EXECUTED
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013277                  7410 *26 TIMES
013277 323 362          7420        OUT  <W2 SET WRITE DATA=00H
013301 323 367          7430        OUT  HALT
013303                  7440 *
013303                  7450 *HEAD IS WRITING FIRST OF 6 00 BYTES
013303 323 367          7460        OUT  HALT
013305                  7470 *2ND OF 6
013305 323 367          7480        OUT  HALT
013307                  7490 *3RD OF 6
013307 323 367          7500        OUT  HALT
013311                  7510 *4TH OF 6
013311 323 367          7520        OUT  HALT
013313                  7530 *5TH OF 6
013313 006 376          7540        LD   B,0FEH LOAD ID MARK IN B
013315 016 062          7550        LD   C,<W3STT+W3CCG+W3WES SET CCG CMND TO C
013317                  7560 *(ALSO RESETS IXS)
013317 026 270          7570        LD   D,<W1CBS+<W1CBN STORE FF CLOCK PATTERN TO D
013321 036 060          7580        LD   E,<W3STT+W3WES STORE RESET CCG IN E
013323 076 200          7590        LD   A,<W1CBS+<W1CBD "C7" DATA MARK CLOCK PATTERN
013325 323 367          7600        OUT  HALT
013327                  7610 *
013327                  7620 *HEAD IS WRITING 6TH OF 6 00 GAP BYTES
013327 323 361          7630        OUT  <W1 SET "C7"DATA MARK CLOCK PATTERN
013331 170              7640        LD   A,B SET "FE" DATA BITS
013332 323 362          7650        OUT  <W2 FOR ID MARK
013334 171              7660        LD   A,C SET CCG THIS CAUSES CRC
013335 323 363          7670        OUT  <W3 CALCULATION TO BEGIN AT NEXT BRP
013337 172              7680        LD   A,D GET "FF" DATA CLOCK BIT PATTERN
013340 323 367          7690        OUT  HALT
013342                  7700 *
013342                  7710 *HEAD IS WRITING ID ADDRESS MARK
013342 323 361          7720        OUT  <W1 SET FF DATA CLOCK FOR NEXT BYTE.
013344 173              7730        LD   A,E RESET CCG.
013345 323 363          7740        OUT  <W3
013347                  7750 *CRC MUST BE RESET BEFORE NEXT BRP OR CRC CALCULATION
013347                  7760 *WOULD BEGIN AGAIN
013347 174              7770        LD   A,H LOAD TRACK ADDRESS
013350 323 362          7780        OUT  <W2
013352 323 367          7790        OUT  HALT
013354                  7800 *HEAD IS WRITING TRACK ADDRESS
013354 257              7810        XOR  A
013355 323 362          7820        OUT  <W2 1ST ZERO BYTE
013357 323 367          7830        OUT  HALT
013361                  7840 *HEAD IS WRITING FIRST ZERO BYTE
013361 175              7850        LD   A,L
013362 323 362          7860        OUT  <W2 SET DATA BYTE=SECTOR ADDRESS
013364 323 367          7870        OUT  HALT
013366                  7880 *HEAD IS WRITING SECTOR ADDRESS
013366 257              7890        XOR  A
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013367 323 362          7900        OUT  <W2 2ND ZERO BYTE
013371 323 367          7910        OUT  HALT
013373                  7920 *HEAD IS WRITING 2ND ZERO BYTE
013373 076 061          7930        LD   A,<W3STT+W3CCW+W3WES SET CCW; IN WRITE MODE
013375                  7940 *WILL BEGIN WRITING BITS FROM THE CRC REGISTERS AT NEXT
013375                  7950 *BRP FOLLOWING THE SETTING OF CCW
013375 323 363          7960        OUT  <W3
013377 323 367          7970        OUT  HALT
014001                  7980 *HEAD IS WRITING FIRST CRC BYTE
014001 323 367          7990        OUT  HALT
014003                  8000 *HEAD IS WRITING 2ND CRC BYTE
014003 076 377          8010        LD   A,0FFH LOAD "FF" GAP BYTE IN WRITE DATA REG
014005 323 362          8020        OUT  <W2
014007 076 060          8030        LD   A,W3STT+W3WES RESET CCW; BIT WRITING
014011 323 363          8040        OUT  <W3 WILL STOP AT NEXT BRP
014013 006 013          8050        LD   B,11D B= BYTE COUNT
014015 323 367          8060        OUT  HALT
014017 323 367          8070 FM080  OUT  HALT
014021                  8080 *HEAD WRITES GAP BYTES 1 THROUGH 11
014021 005              8090        DEC  B DONE?
014022 040 373          8100        JR   NZ,FM080 NO, REPEAT
014024 257              8110        XOR  A YES, CHANGE GAP BYTE
014025 323 362          8120        OUT  <W2 TO 00H
014027 323 367          8130        OUT  HALT
014031                  8140 *BYTE 12
014031 323 367          8150        OUT  HALT
014033                  8160 *BYTE 13
014033 323 367          8170        OUT  HALT
014035                  8180 *BYTE 14
014035 323 367          8190        OUT  HALT
014037                  8200 *BYTE 15
014037 323 367          8210        OUT  HALT
014041                  8220 *HEAD IS WRITING GAP BYTE 16
014041 006 373          8230        LD   B,0FBH LOAD DATA MARK TO B
014043 016 062          8240        LD   C,<W3STT+W3CCG+W3WES SET CCG COMMAND TO C
014045 026 270          8250        LD   D,<W1CBS+<W1CBN STORE FF CLOCK PATTERN
014047 036 040          8260        LD   E,<W3STT
014051 076 200          8270        LD   A,<W1CBS+<W1CBD STORE "C7" DATA MARK CLOCK
014053 323 367          8280        OUT  HALT
014055                  8290 *HEAD IS WRITING GAP BYTE 17
014055 323 361          8300        OUT  <W1 SET C7 DATA MARK CLOCK PATTERN
014057 170              8310        LD   A,B SET "FB" DATA BITS FOR DATA MARK
014060 323 362          8320        OUT  <W2
014062 171              8330        LD   A,C SET CCG. THIS CAUSES CRC CALCULATION TO
014063 323 363          8340        OUT  <W3 BEGIN AT NEXT BRP
014065 172              8350        LD   A,D GET "FF" DATA BIT CLOCK PATTERN CMND
014066 323 367          8360        OUT  HALT
014070                  8370 *
014070                  8380 *HEAD IS WRITING DATA ADDRESS MARK
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014070 323 361          8390        OUT  <W1 SET FF DATA BIT CLOCK FOR NEXT BYTE
014072 173              8400        LD   A,E RESET CCG. CCG MUST BE RESET BEFORE NEXT
014073                  8410 *BRP OR CRC CALCULATION WOULD BEGIN AGAIN
014073 323 363          8420        OUT  <W3
014075 076 345          8430        LD   A,0E5H LOAD DATA
014077 323 362          8440        OUT  <W2
014101 323 367          8450        OUT  HALT
014103                  8460 *HEAD WRITES DATA BYTE 1
014103 006 177          8470        LD   B,<NBSCT-1
014105 323 367          8480 FM100  OUT  HALT
014107                  8490 *
014107                  8500 *HEAD WRITES DATA BYTES 2 THROUGH NBSCT
014107 005              8510        DEC  B
014110 302 105 014      8520        JP   NZ,FM100
014113 076 061          8530        LD   A,<W3STT+<W3CCW+<W3WES SET CCW; IN WRITE CHIP
014115                  8540 *WILL BEGIN WRITING BITS FROM THE CRC REGISTERS AT THE
014115                  8550 *NEXT BRP FOLLOWING THE SETTING OF CCW
014115 323 363          8560        OUT  <W3
014117 323 367          8570        OUT  HALT
014121                  8580 *HEAD IS WRITING FIRST CRC BYTE
014121 323 367          8590        OUT  HALT
014123                  8600 *HEAD IS WRITING 2ND CRC BYTE
014123 076 377          8610        LD   A,0FFH LOAD "FF" GAP BYTE IN WRITE DATA REG
014125 323 362          8620        OUT  <W2
014127 076 060          8630        LD   A,<W3STT+<W3WES RESET CCW; CRC WRITING ENDS
014131 323 363          8640        OUT  <W3
014133 006 033          8650        LD   B,27D B= BYTE COUNT
014135 323 367          8660        OUT  HALT
014137 323 367          8670 FM110  OUT  HALT
014141                  8680 *HEAD WRITES GAP BYTES 1 THROUGH 27
014141 005              8690        DEC  B DONE?
014142 040 373          8700        JR   NZ,FM110 NO, REPEAT
014144 054              8710        INC  L INCREMENT SECTOR ADDRESS
014145 076 032          8720        LD   A,26D
014147 275              8730        CP   L LAST SECTOR?
014150 362 276 013      8740        JP   P,FM070 NO, WRITE ANOTHER SECTOR
014153                  8750 *WRITE FF'S TO END OF TRACK
014153 323 367          8760 FM120  OUT  HALT
014155                  8770 *
014155                  8780 *HEAD WRITES GAP BYTES 28 TO 247
014155 333 360          8790        IN   <R0 READ STATUS
014157 057              8800        CPL
014160 346 002          8810        AND  R0IRQ INDEX REQUEST?
014162 312 153 014      8820        JP   Z,FM120 NO, CONTINUE
014165                  8830 *END OF TRACK
014165 076 004          8840        LD   A,<W3WER
014167 323 363          8850        OUT  <W3 WRITE ENABLE AND STT RESET
014171 333 360          8860        IN   <R0 LOAD STATUS
014173 057              8870        CPL
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014174 346 010          8880        AND  ROERR ERRORS?
014176 040 024          8890        JR   NZ,FM130
014200                  8900 *INDEX REQUEST IS AUTOMATICALLY RESET BY STT RESET
014200 076 114          8910        LD   A,<NTRKS-1
014202 274              8920        CP   H LAST TRACK?
014203 310              8930        RET  Z YES, FORMATTING COMPLETE
014204 056 001          8940        LD   L,01H NO, RESET SECTOR ADDRESS
014206 044              8950        INC  H INCREMENT TRACK ADDRESS
014207 345              8960        PUSH HL SAVE HL
014210 006 002          8970        LD   B,02H WAIT FOR TUNNEL ERASE HEAD
014212 315 131 013      8980        CALL DELAY TO REACH END OF TRACK BEFORE
014215 315 243 012      8990        CALL STI STEPPING HEAD
014220 341              9000        POP  HL RESTORE DATA IN HL
014221 303 172 013      9010        JP   FM030 AND CONTINUE
014224                  9020 *ERROR SERVICE ROUTINE
014224 062 304 014      9030 FM130  LD   (WRITF),A
014227 062 270 014      9040        LD   (MERF),A
014232 303 315 010      9050        JP   ERROR
014235                  9060 ********************************************************
014235                  9070 *TABLES, COUNTERS, POINTERS, ETC.
014235                  9080 *LIMIT TABLE (UPPER AND LOWER FOR PARAMETERS
014235                  9090 LMTBL  DB   1
001
014236                  9100        DB   NU+1 UNIT
002
014237                  9110        DB   0
000
014240                  9120        DB   NTRKS TRACK
115
014241                  9130        DB   1
001
014242                  9140        DB   NSCTR+1 SECTR
033
014243                  9150        DB   4
004
014244                  9160        DB   NBSCT+1 SCTSZ
201
014245                  9170 *------------------------------------------------------
014245                  9180 *COMMAND TABLE
014245                  9190 CTBL   DW   READ  1
  156 011
014247                  9200        DW   WRITE 2
  374 011
014251                  9210        DW   SEEK  3
  206 012
014253                  9220        DW   INIT  4
  076 010
014255                  9230        DW   FRMAT 5
  161 013
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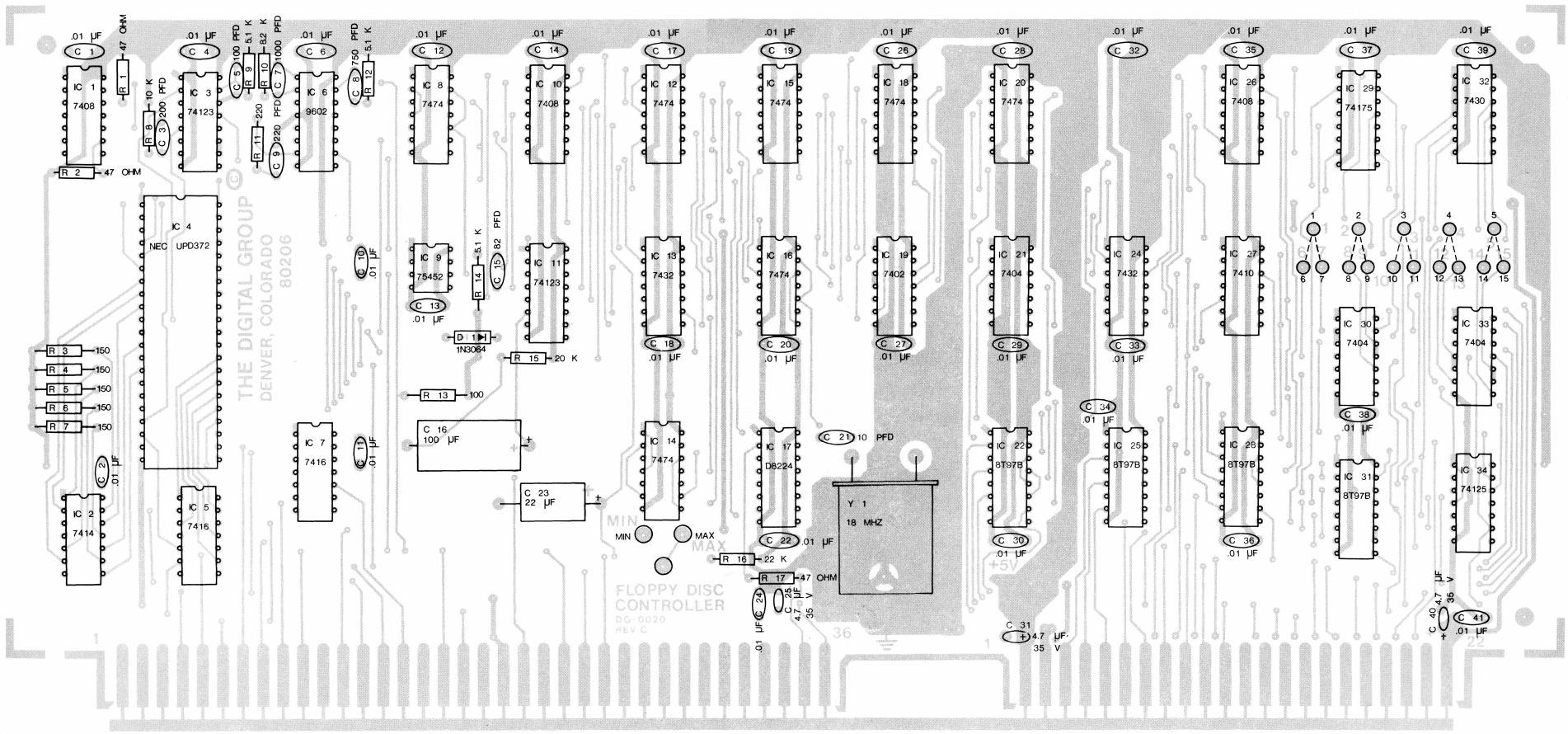
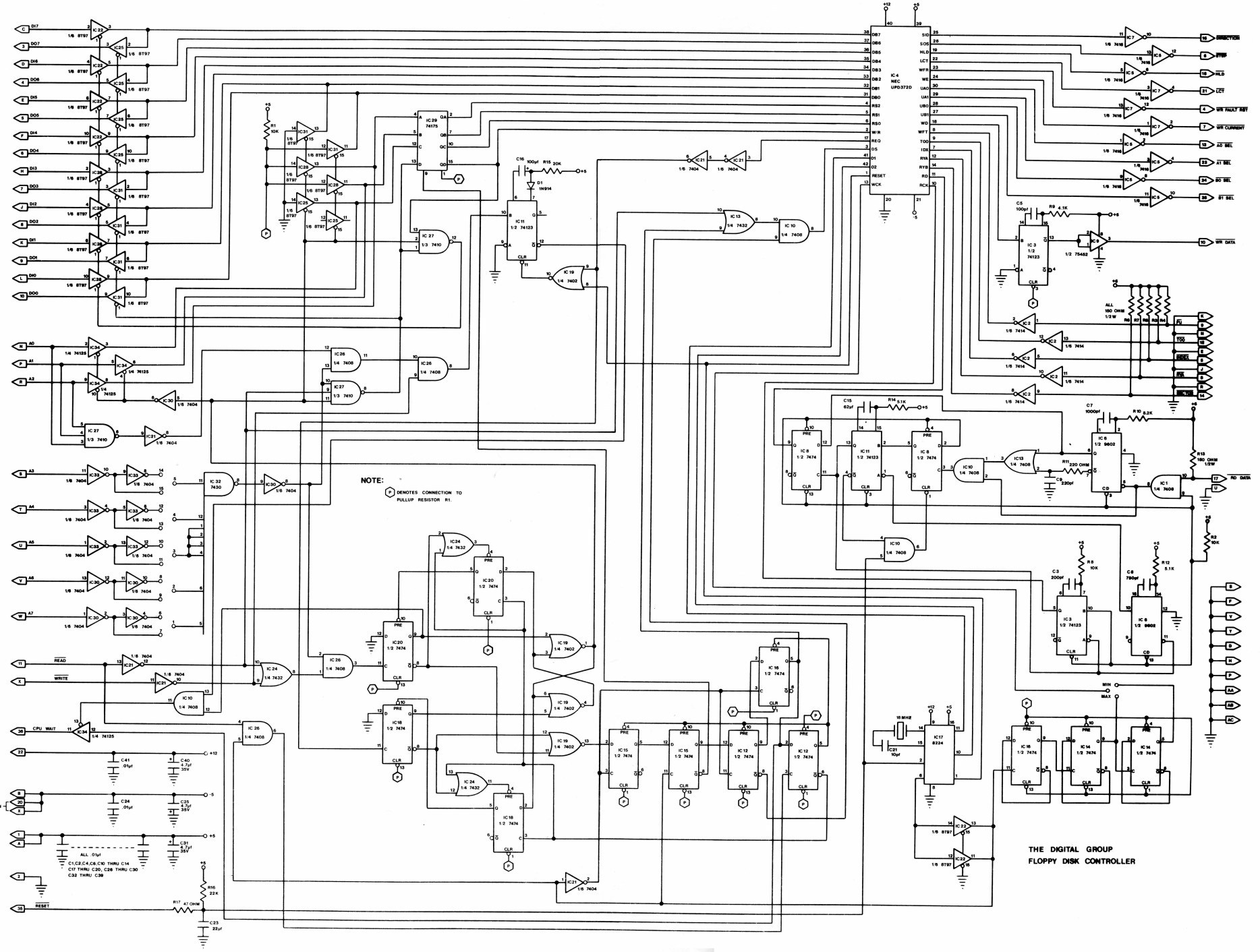
014257                  9240        DW   RSTO  6
  022 010
014261                  9250 *
014261                  9260 NCMDS  EQU  06H
014261                  9270 *-----------------------------------------------------
014261                  9280 BUFFR  DW   BUF THIS IS THE POINTER TO THE DATA
  312 014
014263                  9290 *COMMAND
014263                  9300 CMND   DS   01H COMMAND (1-NCMDS)
014264                  9310 *-----------------------------------------------------
014264                  9320 *PARAMETERS
014264                  9330 UNIT   DS   01H DRIVE NUMBER BEING COMMANDED
014265                  9340 TRACK  DS   01H TRACK DESIRED
014266                  9350 SECTR  DS   01H SECTOR DESIRED
014267                  9360 SCTSZ  DS   01H SECTOR SIZE
014270                  9370 NP     EQU  $-UNIT NUMBER OF PARAMETERS
014270                  9380 *-----------------------------------------------------
014270                  9390 *FLAGS
014270                  9400 MERF   DS   01H MASTER ERROR FLAG
014271                  9410 CMDER  DS   01H COMMAND ERROR
014272                  9420 PRMER  DS   01H PARAMETER ERROR
014273                  9430 SLCTF  DS   01H SELECT FAULT (DRIVE DID NOT COME READY)
014274                  9440 NOGO   DS   01H FAILED TO FIND SECTOR FLAG
014275                  9450 WTRK   DS   01H WRONG TRACK
014276                  9460 ZERO1  DS   01H ZERO BYTE 1 NOT ZERO
014277                  9470 ZERO2  DS   01H ZERO BYTE 2 NOT ZERO
014300                  9480 CRCID  DS   01H CRC ERROR IN ID
014301                  9490 CRCDR  DS   01H CRC ERROR IN DATA READ
014302                  9500 ILLMK  DS   01H ILLEGAL DATA MARK FLAG
014303                  9510 DELMK  DS   01H DELETED DATA MARK FLAG
014304                  9520 WRITF  DS   01H WRITE FAULT
014305                  9530 NF     EQU  $-MERF NUMBER OF FLAGS
014305                  9540 *-----------------------------------------------------
014305                  9550 *COUNTERS, POINTERS, STATUSES
014305                  9560 RRTRY  DS   01H READ RETRY COUNTER
014306                  9570 WRO    DS   NU COPIES OF LATEST WO
014307                  9580 TKPTR  DS   NU TRACK POINTER FOR EACH UNIT
014310                  9590 REVS   DS   NU ELAPSED IDLE REVOLUTIONS
014311                  9600 HEAD   DS   NU HEAD STATUS; 1=LOADED, 0=UNLOADED
014312                  9610 NB     EQU  $-CMND NUMBER OF BYTES IN DATA AREA
014312                  9620 *-----------------------------------------------------
014312                  9630 *
014312                  9640 BUF    DS   NBSCT THIS IS NORMALLY THE DATA BUFFER AREA
015112                  9650 *
015112                  9660        END

FILE  060000  247062
READY
```

FLOPPY DISK CONTROLLER CARD



03-090-046


NOTE:
(P) DENOTES CONNECTION TO PULLUP RESISTOR R1.
ALL 01µf
C1,C2,C4,C6,C10 THRU C14
C17 THRU C20, C26 THRU C30
C33 THRU C39
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