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THE DIGITAL GROUP CASSETTE STORAGE SYSTEM

298-050-3-48+2

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I. INTRODUCTION

The Digital Group Cassette Storage System is a total magnetic tape data storage and retrieval system capable of controlling up to four Phideck cassette transports and accessing any of over one million 8-bit bytes within 20 seconds, using standard C-30 Phillips cassettes.

The system is ideal for general purpose data and program storage, file copying, editing, and sorting operations. Each deck is fully controlled to prevent tape breakage. Electronic braking precisely controls tapes for fast forward and rewind operations. A 4- to 5-bit translation scheme, called Group Coded Recording, allows higher packing densities with a soft error rate of less than one bit in 10^8. This system operates at 1600 flux changes per inch, yielding a data transfer rate of 800 bytes per second at a tape speed of five inches per second.

SPECIFICATIONS

Recording Density:	1600 FCPI (Flux Changes Per Inch)
Data Density:	1280 BPI (Bits Per Inch) using 4- to 5-bit Group Coded Recording
Data Rate:	800 Bytes per second (6400 Baud)
Data Capacity:	250,000 bytes on each side of a C-30 audio cassette 540,000 bytes on each side of 300 foot data cassette
Tape Speed:	5 IPS Read/Write 100 IPS Fast Forward/Reverse
Speed Tolerance:	±15% (i.e., the system will read a tape that was recorded 15% from the nominal speed without adjustment. It will read tapes outside this range by adjusting the data rate control.)
Error Rate:	Soft - less than 1 bit in 10^8 Hard - virtually zero when using the software package supplied with the system and a good quality audio tape
Power:	+5V DC ±5% 1.0 Amps nominal 1 drive 2.0 Amps maximum 4 drives 4.0 Amps peak for .1 second during drive enable +12V DC unregulated (limits: 11V-20V) 0.4 Amp average with tape moving 0.7 Amp peak during motor start

II. SOFTWARE INTERFACE

Since the absolute method of controlling the cassette system will differ for each installation, only a basic interface will be described. The user can then modify the basic interface to meet his own requirements.

COMMANDS

The command port (see Table 2.1) interprets the various commands into tape motion and activates the read/write electronics. The two select bits, SEL1 and SEL2, select the active deck, according to Table 2.2. The selected deck can only be changed when all decks are stopped (status bit NOT BUSY is on). Otherwise, even though a command may specify a different deck, the original deck will be used. ENABLE/DISABLE (Enable=1, Disable=Ø) controls the deck capstan motors so that they may be turned off under software control. The capstan motors should be enabled during and at least one second prior to any other commands. STOP/RUN (Stop=1, Run=Ø) controls tape motion. The STOP command also takes up slack in the tape. FWD/REV (Fwd=1, Rev=Ø) controls tape direction, and SLOW/FAST (Slow=1, Fast=Ø) controls tape speed. Note that since "slow reverse" cannot be performed, a "slow forward" is automatically substituted. RCD/READ (Record=1, Read=Ø) controls the Read/Write electronics, and ERASE (=1) will erase the tape when RCD is selected. All commands other than the RECORD or ERASE commands should have RCD/READ=Ø to prevent recording spurious glitches on the tape.

Table 2.1

STATUS AND COMMAND PORTS

COMMAND PORT

Bit	Definition (1 active)	
Ø	SEL 1	
1	SEL 2	
2	1=ERASE	
3	1=RECORD	Ø=READ
4	1=STOP	Ø=RUN
5	1=FORWARD	Ø=REVERSE
6	1=SLOW	Ø=FAST
7	1=ENABLE	Ø=DISABLE

STATUS PORT

Bit	Definition (1 active)
Ø	OVERRUN/UNDERRUN
1	READY (data ready or ready for data)
2	STOP (possible jam or end of tape)
3	NOT BUSY (user may change decks)

Table 2.2

DECK SELECTION

SEL 2	SEL 1	DECK
Ø	Ø	Ø
Ø	1	1
1	Ø	2
1	1	3

STATUS

The status port (see Table 2.1) provides information on the state of the controller. Four status bits are brought out, leaving four input bits for other uses. Two of the bits, STOP and NOT BUSY, supply information on the deck status. STOP is an immediate response to a stop command or a jam. NOT BUSY occurs about a second after STOP turns on, signifying the deck is totally stopped. STOP is used by the software in all cases, except to switch the selected deck, which can only occur in a not busy state. The other two bits are status bits for the read/write electronics. READY indicates that the deck can accept another data byte (in Record) or that a new data byte is in the DATA-OUT port (in Read). READY is reset about one millisecond after it is set. It is also reset by a command, data in, or data out strobe. OVERRUN/UNDERRUN indicates that the computer has not serviced a READY by supplying or looking at the new character within the required time. It will remain set until a new command is issued. It is to be treated in most cases as an error condition.

INPUT DATA (FOR RECORD)

The data input port requests the data bytes which are to be recorded on the tape. The first byte should be loaded either prior to issuing the record command or within about five milliseconds after issuing the record command. Each subsequent byte of data to be recorded should be loaded when the READY status goes high. Loading the new byte will automatically reset the READY line. The byte should be loaded within .5 milliseconds after the READY signal. Otherwise, OVERRUN/UNDERRUN will come on, and the record electronics will go into erase mode. This may be allowed to happen at the end of a data block in order to record an inter-record gap. If a new command is to be given immediately after the last recorded byte, the OVERRUN/UNDERRUN bit must come on before the command is given. If the command is issued earlier, part of the last byte will not be recorded.

OUTPUT DATA (FOR READ)

The data output port is loaded by the read/write electronics with the data being read from the tape. After issuing a read command, the electronics will look for a sync pattern and then load the output port with the first data byte. At this time, READY will go high. When the byte is read, the READY signal will be reset. The byte should be read within .5 milliseconds after the READY signal. Otherwise, OVERRUN/UNDERRUN will come on, and the read electronics will be halted until another read command is issued.

MECHANICAL CONSIDERATIONS

Since the various tape and head movements require certain amounts of time to stabilize, consideration must be given by the software to insure error free read and record operations.

1. Never issue a record command (or turn on the record bit) when the tape is in any state other than slow forward, and the tape is stabilized against the head. The tape may take as much as one second to align itself with the tape guides on the head, and an unaligned tape may record errors. A good practice to insure reliable recording is to read the previous block without error. This implies the tape is tracking correctly for the record operation.

2. When issuing a read command which causes the head to come up against the tape, noise and random patterns as the tape becomes aligned may cause false synchronizing and give erroneous read data. Therefore, it is good practice in this situation to wait about a second, and then reissue the read command, using only the data from this second read command.

3. When recording the first block of data at the start of a tape, issue an erase command, and then time out about five to seven seconds to allow the tape leader to pass before recording data.

4. To allow the recording of two consecutive blocks at different points in time, always go into erase mode after recording the first block for a time longer than the space between blocks. (This is easily done by ignoring the READY after the last byte has been recorded, and timing out for the erase time. The electronics will immediately begin erasing without glitching). When the block is to be recorded, it is begun somewhere within the erased section, thus preventing any glitching and subsequent false synchronizing on read operations.

The following bit patterns are recommended for issuing the various commands:

COMMAND Bit:	7	6	5	4	3	2	1	Ø
STOP	1	1	1	1	Ø	Ø	Selected Deck	
FAST FORWARD	1	Ø	1	Ø	Ø	Ø	(Note: Selected	
FAST REVERSE	1	Ø	Ø	Ø	Ø	Ø	deck may only	
READ	1	1	1	Ø	Ø	Ø	be changed	
RECORD	1	1	1	Ø	1	Ø	when status bit	
ERASE	1	1	1	Ø	1	1	NOT BUSY is on.)	
STANDBY	Ø	1	1	1	Ø	Ø		

III. HARDWARE INTERFACE

Computer Interface

The basic interface of the cassette controller to the computer occurs through four controller I/O ports. These ports may be connected in various schemes to fully utilize the hardware arrangement of the computer.

The computer's output ports connect to the command port and the data-in port. The computer's input ports interface to the data-out port and the status port. Each port has its own strobe line which is used either to strobe information into the internal latch or to activate the tri-state output in order to read the port.

All outputs from the controller will support ten TTL loads, and all data or control inputs are one TTL load, the command strobe is two TTL loads, the data-in strobe is three TTL loads, the status strobe is four TTL loads, and data-out strobe is five TTL loads. The data-out and status ports are tri-state, activated by their respective strobes. All strobe signals are active low, and should remain high when not in use. The command data-in and the data-out strobes should be low for a period greater than 500nsec, but less than one millisecond. A strobe greater than one millisecond is likely to cause false status indication from the read/write electronics.

Some typical connections are shown in Figures 3.1 - 3.3. Figure 3.1 depicts a setup where all input and output ports are provided by the computer. Unless all strobes are obtainable from the computer, a third output port will have to be dedicated for software controlled strobe pulses. The scheme in Figure 3.2 uses this strobe port, but takes advantage of a bus system, since the strobes are no longer tied to specific ports but are under software control. Figure 3.3 uses a bus system found on more complex systems. Here, inputs and outputs are shared on the same line and controlled totally by the strobe signals. **Care should be taken when using this method not to load the bus beyond its capacity.**

Deck Interface

The cassette controller must also be interfaced to the decks. Refer to Figure 5.1 for the wiring of the decks. The board has four separate connections for each of four decks on all pins except ALLCAP, CAPSUPPLY, ALLENGSW, and ALLENGSWGND. The connectors supplied with the deck cables (when decks are included with the controller) will plug into connections for decks Ø and 1. When decks 2 and/or 3 are used, the above signals must be wired into the connector for deck Ø or 1. Also, HDGND is a common head ground, and all cable shields must be terminated at these two pins.

For users with a Digital Group system, refer to the section labeled *Using the Controller in a Digital Group System* following the construction section.

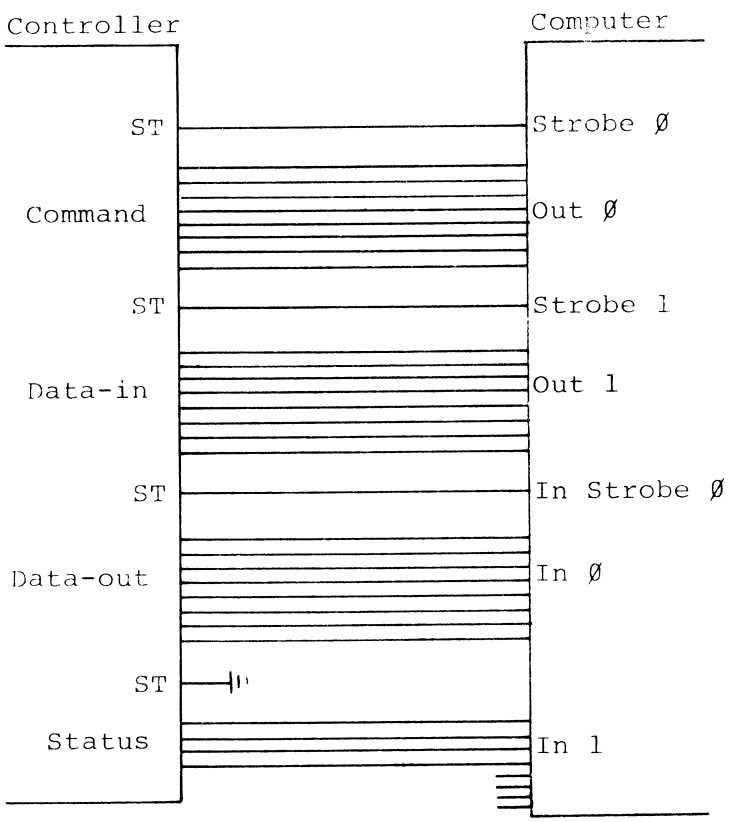


Figure 3.1

DEDICATED I/O PORTS

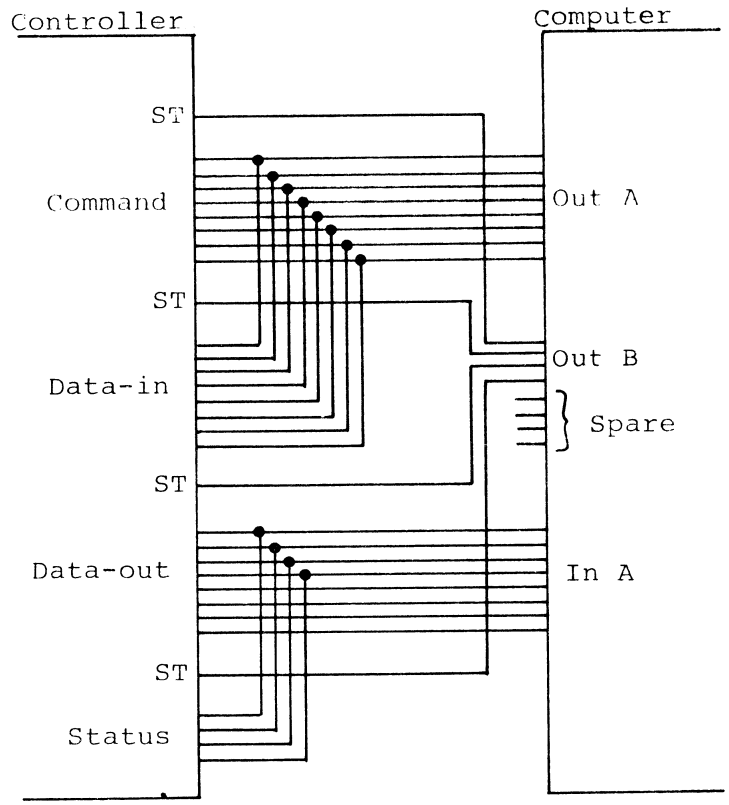


Figure 3.2

MULTIPLEXED I/O PORTS WITH DEDICATED STROBE
(used with Digital Group systems)

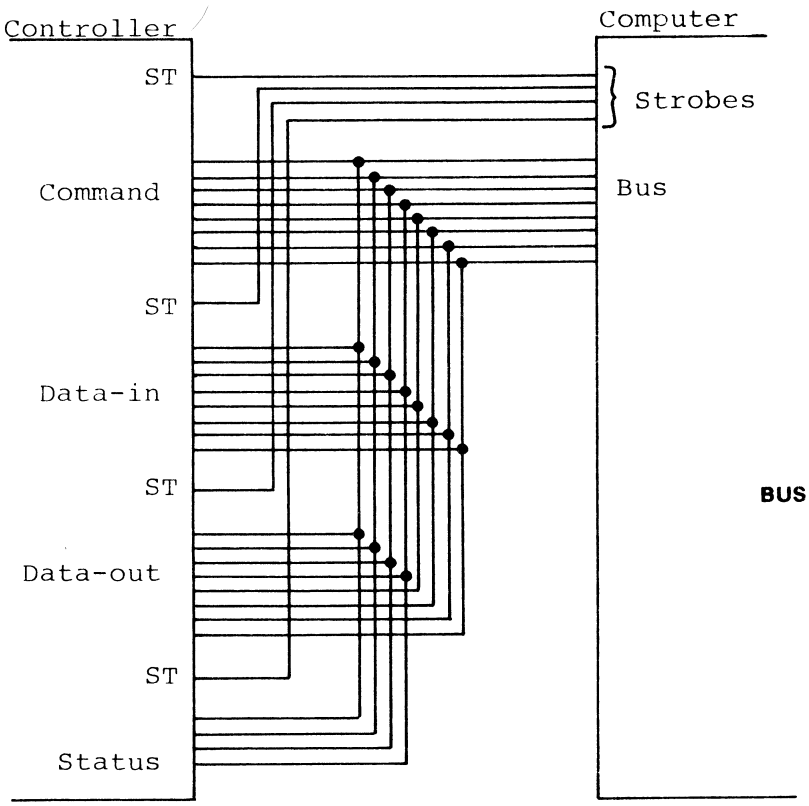


Figure 3.3

BUS ORIENTED PORTS

IV. THEORY OF OPERATION

HEAD ELECTRONICS

The head electronics consists of IC27 and IC28 which drive the head during record and IC13 which amplifies the read signal during read. IC27 and IC28 (75125's) have tri-state outputs which normally are in the high impedance state during a read operation so that they won't influence the low level signal going from the head to the amplifier (IC13). During record, only the sections of IC27 and IC28 associated with the selected drive go into a low impedance state and drive the head in a push-pull manner. R6, R9, R20, and R23 are used to limit the current through the head and should be adjusted for a current of 1.5 times the head saturation current if the standard head is not used. Figure 4.1 shows typical waveforms for the record drivers.

During a read operation, section 1 of IC13 is used as a pre-amp with balanced inputs and a gain of 3.9. Section 2 is an amplifier with a gain of 22. Section 3 is a low-pass filter and differentiator which produces zero crossings at its output whenever the input signal has a peak. The low-pass filter reduces the differentiator's sensitivity to noise. Section 4 is a Schmitt trigger which detects the zero crossings and produces a TTL compatible signal at its output. Figure 4.2 shows typical waveforms for the read electronics.

BIT SYNCHRONIZING ELECTRONICS

This section of the controller is used to generate the proper fixed frequency clocks for record and variable frequency clocks synchronized to the data during read. The data is also converted from NRZI encoding to level encoding. This section of the electronics consists of IC9, IC37, IC50, IC41, IC42, IC55, IC10, IC11, T13, and associated logic and components.

IC9 oscillates at 14 times the bit rate (it takes ten of these bits for every eight bit data byte that is recorded) and is adjusted using R28. During read, IC37 and its associated reset circuitry divides the OSC signal by 8 if the data is coming in slow, by 7 if the data is coming in on frequency, and by 6 if the data is coming in fast. The incoming data rate is checked every time there is a data bit of value "1". There is no correction for data bits of value "Ø". This compensates for small rapid variations in tape speed. Large speed variations generate a DC error voltage with IC10 and IC11 which is fed back to the control input of oscillator IC9. During record, IC37 divides OSC by 7 and T13 turns off the DC feedback loop.

GROUP CODED RECORDING

Since a flux density of 1,600 flux changes per inch was incorporated, a special effort was made to also increase bit density in a packing scheme which maintains self-synchronization. Figure 4.4 illustrates this convention, group-coded recording, in a comparsion with some older methods.

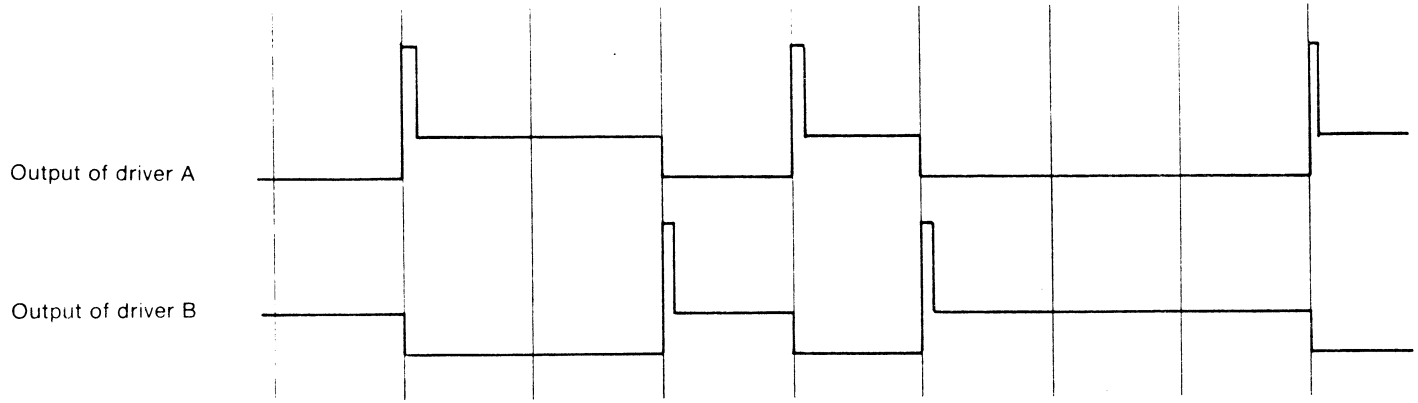


Figure 4.1 Head Electronics Waveforms During a Write Operation

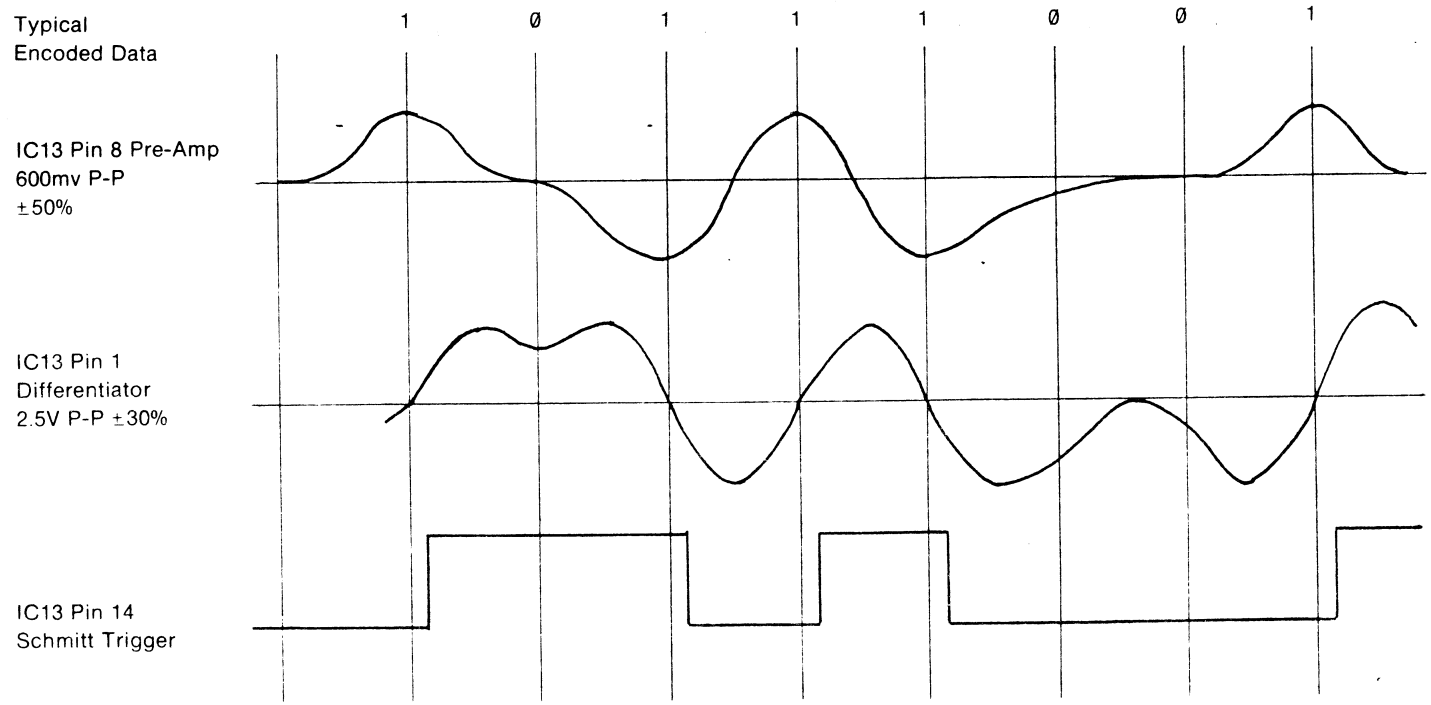
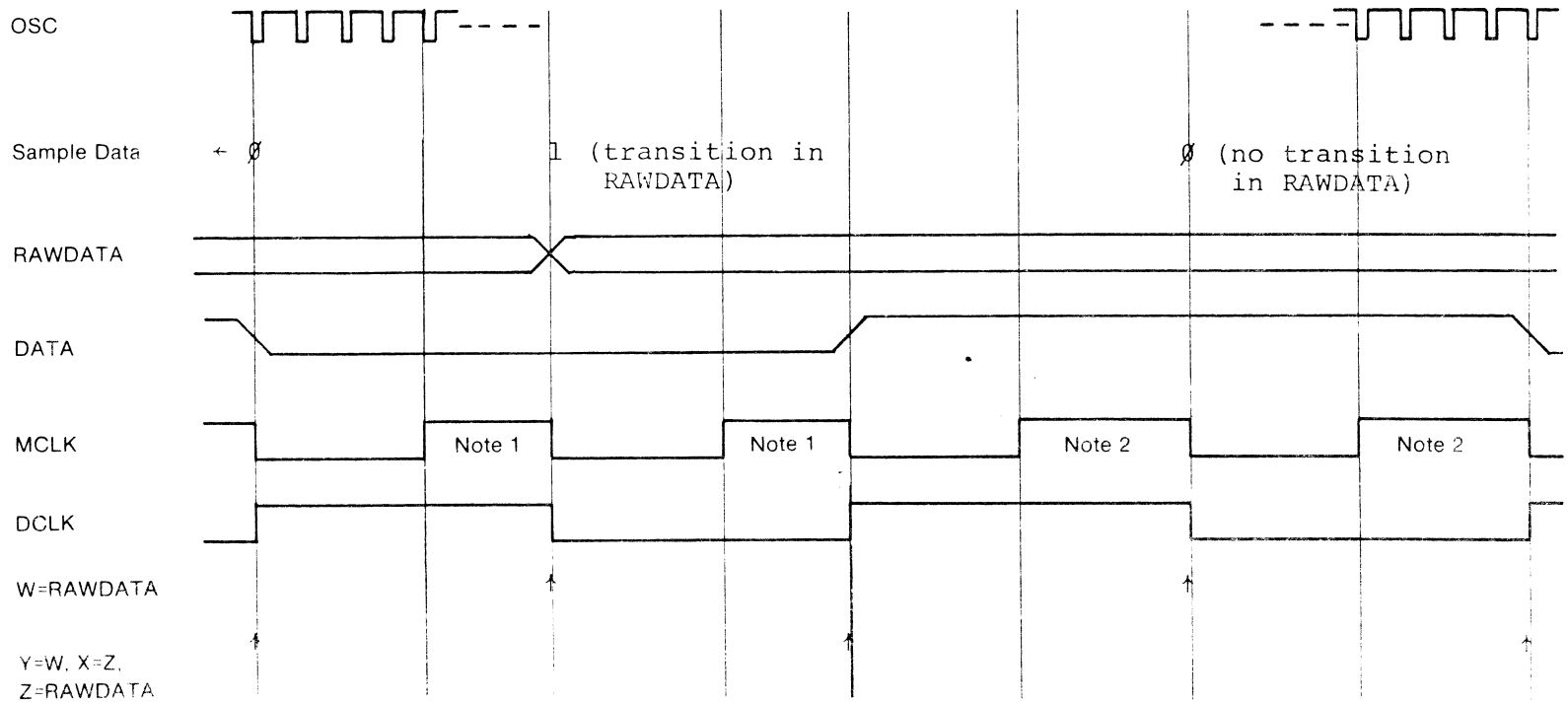


Figure 4.2 Head Electronics Waveforms During a Read Operation



Note 1: This pulse is always 3 OSC cycles if DATA is Ø or RECORDING.

Note 2: This pulse is either 2 or 4 OSC cycles if incoming data is fast or slow respectively and DATA is 1.

Figure 4.3 Bit Synchronizer Timing

NRZI, non-return-to-zero, illustrates a recording efficiency of 1.0, where recording efficiency is defined as the highest ratio of BPI (bits per inch) to FCPI for a given format. There is, at most, only one flux change per bit. Unfortunately, this is not a self-clocking scheme, and is therefore impractical for use on a cassette system which has inherent speed fluctuations.

PE, phase encoding, was designed to overcome such limitations by providing a flux change at the center of each bit period which would synchronize a clocking circuit. The direction of this flux change indicates whether the bit is a 1 or Ø. The recording efficiency of this method, however, is only Ø.5.

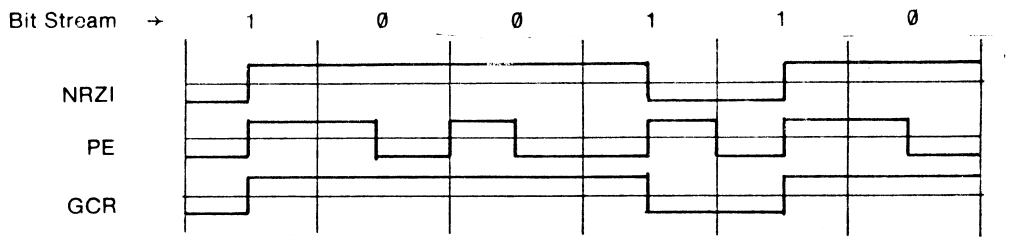


Figure 4.4 Recording Methods

GCR, group-coded recording, at first glance appears very similar to the efficient NRZI method, but with one important difference: No more than two zeros may appear in a row in the bit stream. This guarantees a clock pulse at least once every three bits which provides synchronization. Since a restriction of no more than two zeros in a row cannot be placed on data, a translation scheme is used to encode 4-bit groups into 5-bit groups, and the above restriction is then placed on the 5-bit groups. The translation table is shown in Table 4.5. Since the format is essentially NRZI, we have 4 bits per 5 flux changes, or a recording efficiency of 0.8, which is 60% better than PE.

Table 4.5

4- to 5-Bit Translation Table

4-Bit Data Value	5-Bit Recording Value
0 0 0 0	1 1 0 0 1
0 0 0 1	1 1 0 1 1
0 0 1 0	1 0 0 1 0
0 0 1 1	1 0 0 1 1
0 1 0 0	1 1 1 0 1
0 1 0 1	1 0 1 0 1
0 1 1 0	1 0 1 1 0
0 1 1 1	1 0 1 1 1
1 0 0 0	1 1 0 1 0
1 0 0 1	0 1 0 0 1
1 0 1 0	0 1 0 1 0
1 0 1 1	0 1 0 1 1
1 1 0 0	1 1 1 1 0
1 1 0 1	0 1 1 0 1
1 1 1 0	0 1 1 1 0
1 1 1 1	0 1 1 1 1

RECORDING FORMAT

A synchronous format is automatically added by the electronics to the data being recorded. Of all the 5-bit patterns possible for use in this system, the only pattern not used is 11111. Therefore, this pattern is sent 15 times at the beginning of a data block (75 ones). The purpose of using this pattern is twofold. First, since the start of a block must be found by dropping the head anywhere on the tape, the electronics searches for about 20 ones in a row, and this pattern only occurs at the block start. Second, the ones form a steady clock frequency and allows the self-correcting clocking circuitry to achieve sync in the fastest possible time.

After the ones are recorded, the five bit sequence, 00101, is recorded as a sync character. This particular sequence uniquely defines the absolute start of the block. At this point, the 4 high bits of the first byte are translated to 5 bits and recorded, and then the 4 low bits are translated and recorded. The rest of the bytes are recorded in a similar manner. If a new block is not immediately started, an erase signal will begin after the last byte. Figure 4.6 depicts the format.

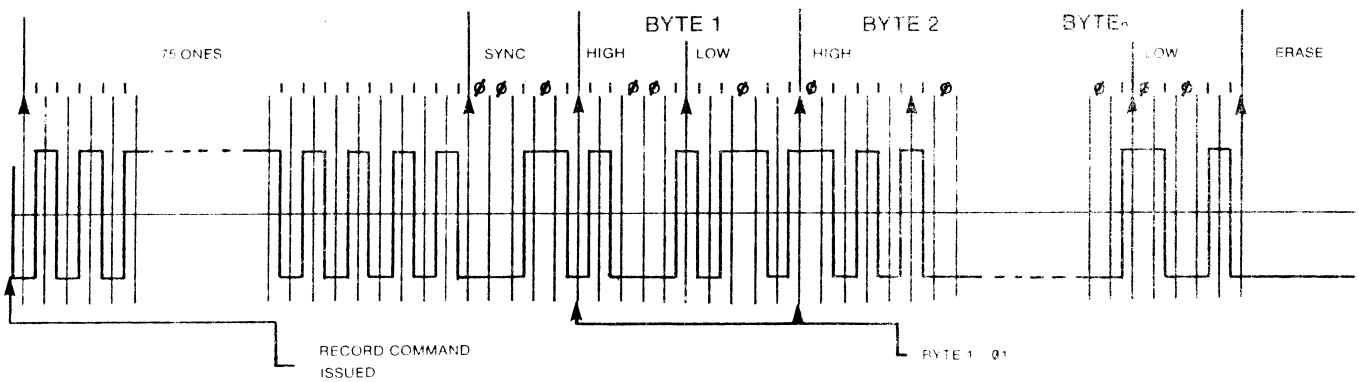


Figure 4.6 Recording Format

DATA FLOW

Record — Data is strobed into IC46 and IC47 with the data input strobe. IC31 and IC32 select the half-byte to be recorded as well as the sync address. IC29 is a ROM which then encodes the 4-bit code into the 5-bit code and sends it to the 5-bit shift register, IC's 30, 5, and 24. The data is then shifted into IC4 which provides the record signal.

Read — Data from the read circuitry is clocked into the 5-bit shift register (IC's 30, 5, and 24). After each half-byte is loaded, data is routed through the selector (IC's 31 and 32) and into the ROM decoder (IC29). Here, the 5-bit code is decoded back into 4 bits and is loaded alternately into IC43 and IC44 to be strobed out.

CONTROL SEQUENCER

The flip-flops whose outputs are RECORD, RUN, B, and A control the sequence of events in the reading and recording processes. Refer to Table 4.7 for the valid sequencer states. The command strobe forces the "SEARCH FOR ONES" state immediately, and system clocks put the sequencer through the appropriate states when the strobe is removed.

For record mode, the sequencer will go to the "GENERATE ONES" state at the next CLOCK1 pulse. The system then waits for IC's 7 and 20 to count out 75 ones and produce the $\overline{\text{ONESDONE}}$ signal. During this time, the ONES signal forces IC29's chip enable to output all ones into the shift register. After the ones are recorded, "SEND SYNC" is entered which produces the $\overline{\text{SYNC-GEN}}$ signal to load a sync pattern into the shift register. Next, "RECORD A" is entered and selects the high bits of the data byte, loading them into the shift register. Finally, "RECORD B" loads and sends the low bits of the data byte. "RECORD A" and "RECORD B" are then alternately repeated until either the next command strobe, a tape stop or jam, or an underrun condition. The latter two events will force the sequencer to the "GAP" or erase state.

Table 4.7

Valid Sequencer States

Function	RECORD	State RUN	B	A
GAP	1	Ø	Ø	1
GENERATES ONES	1	1	Ø	1
RECORD A	1	1	1	1
RECORD B	1	1	1	Ø
SEND SYNC	1	1	Ø	Ø
SEARCH FOR ONES	Ø	Ø	Ø	1
SEARCH FOR SYNC	Ø	1	Ø	1
READ A	Ø	1	1	1
READ B	Ø	1	1	Ø

For read mode, the sequencer remains in the "SEARCH FOR ONES" state until IC's 7 and 20 detect about 20 consecutive ones. If a zero occurs, IC7 is reset and the count begins again. When sufficient ones are found, ONEDET tells the sequencer to go to the "SEARCH FOR SYNC" state. Each read bit is then shifted into IC30 and all five bits in the shift register are selected and routed to the ROM. The SYNC signal occurs when the proper sync bit pattern is found. The "reset to 9" on IC20 is then released and the sequencer is synchronized to the data. Also, the "READ A" state becomes active, and the next five bits of data are shifted in, decoded, and loaded into IC43 as "READ B" is activated. The next five bits are operated on in the same way, except that IC44 is now loaded, and the sequencer goes back to state "READ A".

This sequence repeats until either a command strobe or an overrun occurs. In the second case, the "SEARCH FOR ONES" state is again forced until the next command strobe.

DATA STATUS LOGIC

READY and OVERRUN/UNDERRUN are controlled by IC21 and only occur at the times the shift register or the data output latches are being loaded. READY is set at the end of state "RECORD B" as the second half-byte of data is loaded into the shift register. It must then be serviced by the time "RECORD A" is entered, since the new first half-byte of data is needed at that point. If READY is not reset at this point (by the input data strobe), OVERRUN/UNDERRUN will latch on.

In read mode, READY is set at the end of state "READ B". It is at this time that the second half-byte of data is loaded into IC44. If the output data byte is not read before the next half-byte is loaded, the OVERRUN/UNDERRUN flag is latched on.

CLOCKS AND SYSTEM TIMING

There are four major clocking signals derived from a four-phase clock system. MCLK, the master clock, with DCLK, the data clock, generate ECLK, as in Figure 4.8.

IC20 is used to divide DCLK by 5 and get a signal, DIVIDE-BY-5, once every data half-byte. This is combined with other clock phases and sequencer states to obtain the clocks and signals shown in Figure 4.9.

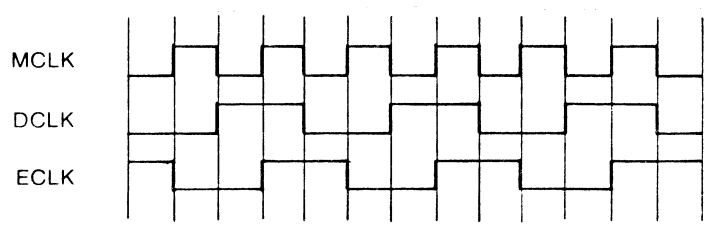
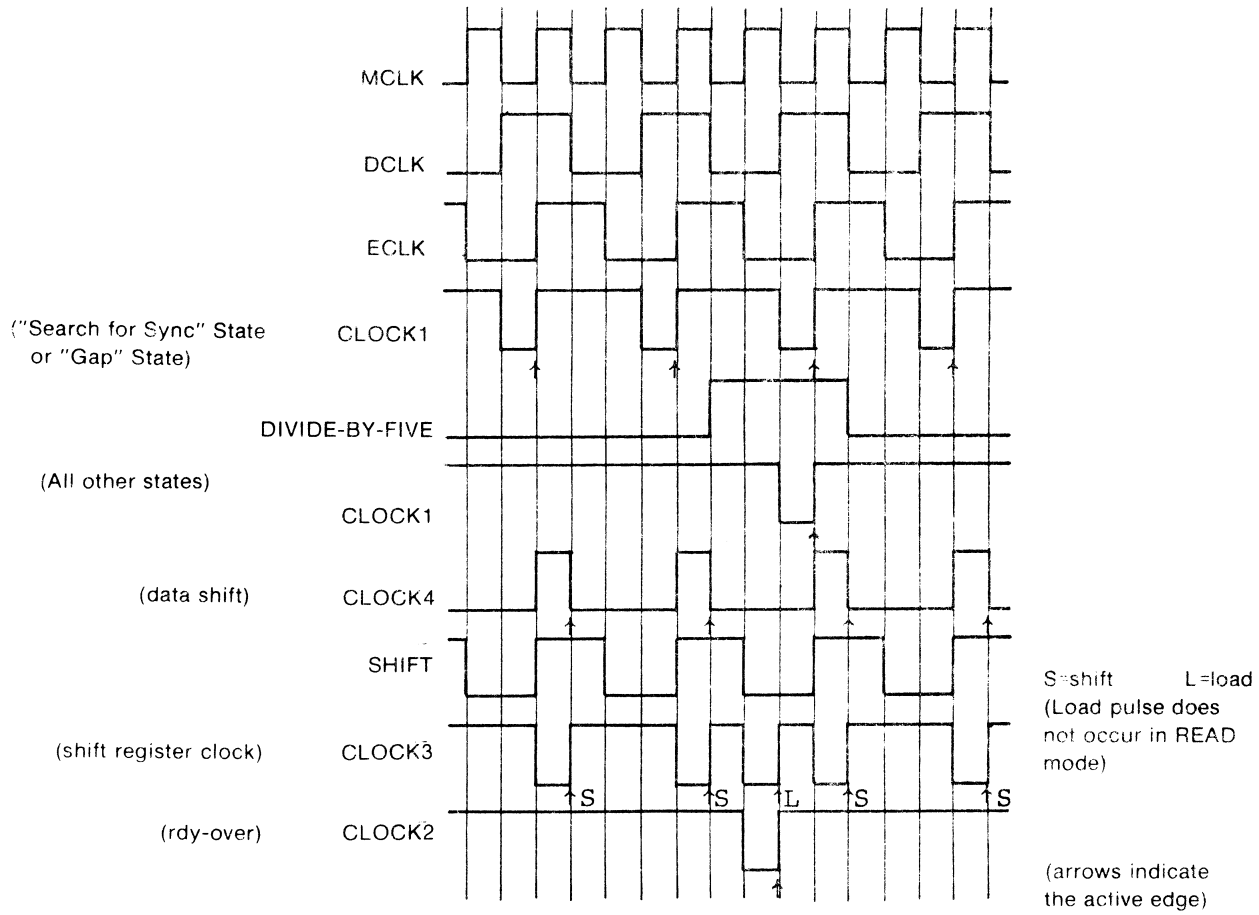


Figure 4.8 4-Phase Clocks

Figure 4.9 System Clock Signals



MOTOR DRIVE AND SENSE ELECTRONICS

The purpose of this section of the controls is to provide drive to the motors, braking for the motors, deck selection, and sense tape motion for feedback to the motor control electronics.

TAKUPDRV goes to the low state whenever the takeup reel should be driven during read or record. R46 limits the motor torque during this operation. BOTHDRV goes low whenever the motor control electronics senses that the reels should have braking torque applied or that there may be slack in the cartridge. R45 limits the torque during this operation. ALCAP is used to turn on the capstan drive motor.

ENGAJDRV goes to the low state whenever the motor control electronics senses that the head and pinch roller should be moved toward or away from the tape. T7, T8, T9, and T10 are used to brake the engage motor whenever it is not being driven. FFDRV and FRDRV are used to drive the tape in the fast forward or fast reverse direction whenever those commands are given.

Transistors T2, T3, T4, and T5 in conjunction with steering diodes D1-D11 and D15 are used to provide drive to the selected deck. Diodes D12, D13, and D14 apply drag to the undriven reel during the fast forward and reverse operations to prevent excessive tape speed and to slow the tape as it nears the end of the reel. Transistors T11 and T12 generate a signal called SPIN which tells the motor control electronics that the undriven reel is turning during the fast forward and reverse operations. The PULSE signal has small negative going pulses on it whenever the takeup reel is turning. This is used to detect tape jams and end of tape during the read, record, or erase operations.

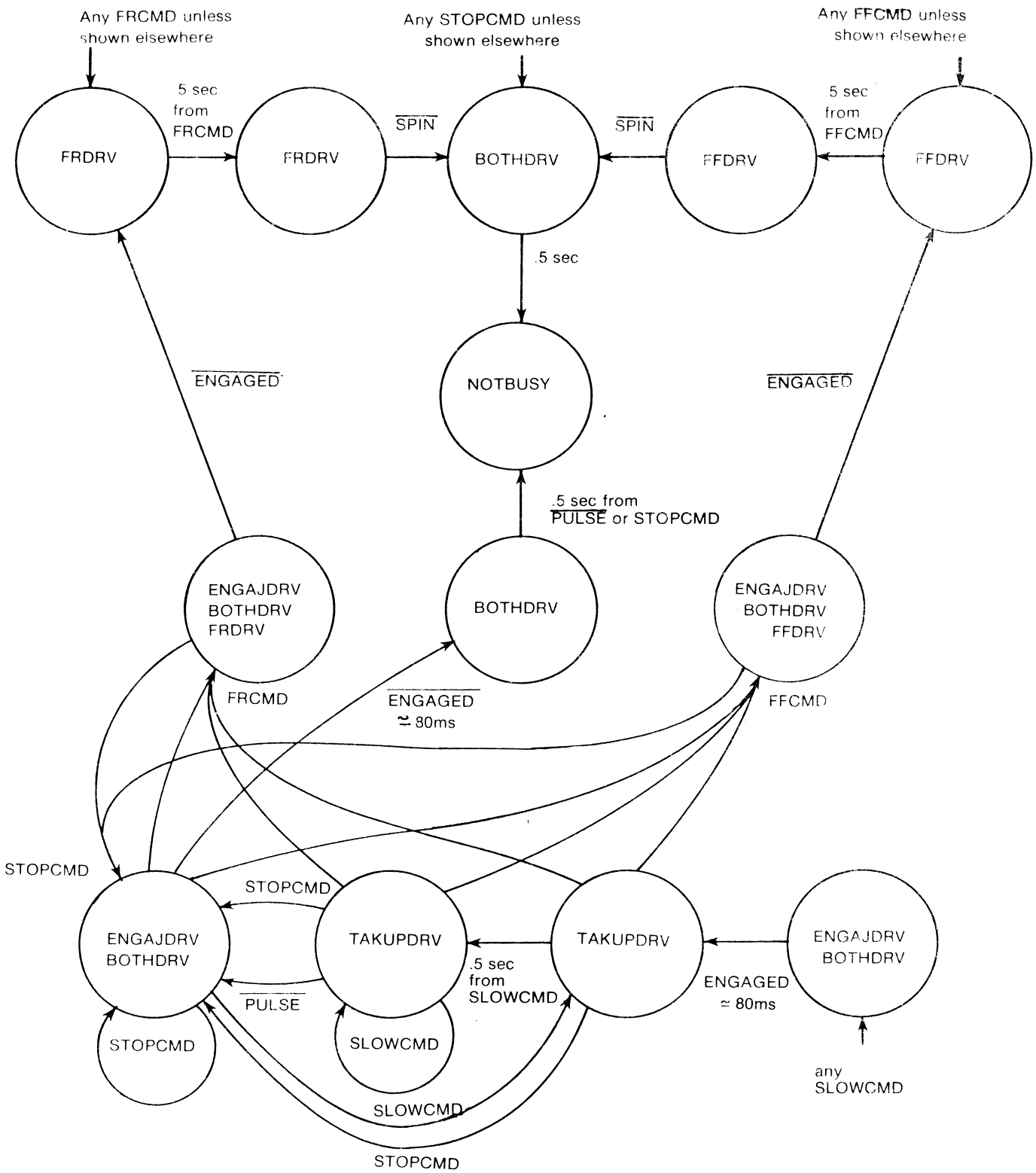
MOTOR CONTROL ELECTRONICS

The motor control electronics senses the status of the tape motion, the position of the headbar, and the commands given by the user and sends control signals to the motor drive circuits. The status bits STOP and NOT BUSY are also generated and sent to the user interface.

The following discussion provides the user with a description of the primary control signals. The user should look at the state diagram given in Figure 4.10 to determine how the deck is actually controlled.

PULSES is generated by a one-shot (IC23) that goes active whenever a command is given and the deck is in the stopped state. PULSES stays active as long as a pulse is received on the PULSE line at least once every half second. If a pulse is not received within the allowed time, $\overline{\text{PULSES}}$ will go to a 1 and cause the deck to go toward the NOT BUSY state. The DELAY signal is also generated by a one-shot (IC23) and is used to inhibit tape motion sensing for ½ second after a command is given to allow for the tape to accelerate to the proper speed. This one-shot is also used to time the BOTH signal after a STOP command or tape jam is detected.

QUIT will go to the 1 level if the manual stop button is pressed, if a STOP command is given, if no pulses are detected and there is an active SLOW command, or if SPIN goes low during any FAST command and DELAY is not active. QUIT is equivalent to STOP on the user interface.



Note: Names within circles are motor control signals. Labels on lines indicate commands given by user or events within controller.

Figure 4.10 Motor Control State Diagram

V. CONSTRUCTION

Tools: Fine tipped, low wattage soldering iron, "wire solder" (around 20 gauge resin solder), small diagonal cutters, needle-nose pliers.

Test Equipment: Voltmeter
500KHz or better oscilloscope
Frequency counter
Microprocessor, Mini, etc.

Estimated Construction Time:
6-11 hours

1. Using the component placement chart given in the appendix, insert the 12 16-pin sockets into the PC board. If the sockets have an indicator for pin one, orient it away from the edge connector. Invert the board by placing a book on the sockets to hold them in and **carefully** solder all pins.
2. Insert and solder the 36 14-pin sockets as described above.
3. Insert and solder the 6 8-pin sockets.
4. The controller and deck need +5 Volts at 1 Amp nominal and +12 Volts at 0.7 Amps peak. Insert IC12, using silicone grease and the heat sink. Solder R57 and R58.
5. Apply power to the board and check voltages at the traces labeled 9V and 5V. The 9 Volt supply should be between 8.4 and 9.6 Volts. The 5 Volts should be between 4.75 and 5.25.
6. Remove power from the board.
7. Insert and solder the three resistors rated above ¼ watt (R44, R45, and R46).
8. Insert and solder the data-rate potentiometer (R28). Orient it so that it may be adjusted from the top of the board.
9. Insert and solder the remaining resistors.
10. Insert and solder all polarized capacitors (C2, C13-C19, C22, C27, C30, C32, C33). C13 and C14 are marked with a + or –. The others have a solid section of color on the positive lead. The board has + notations to aid in orientation.
11. Insert and solder the various remaining capacitors.
12. Insert and solder the four 1N4148 diodes and the 15 1N4001 diodes. All diodes should be oriented so that the bands on the diode are toward the right side of the board. There is also a diode symbol in the board to aid in orientation.
13. Insert and solder T6-T12 into place. **The emitter lead for these transistors is marked with a dot on one of the transistor pads.** The appendix contains a pictorial to aid in orienting the various transistors supplied in your kit.
14. Insert and solder the FET (T13). Orient it so that the drain is toward the top of the board (opposite from the connector).
15. Insert and solder T1-T5. These transistors are placed vertically with the leads inserted fully through the circuit board. **Note that the emitter lead is marked with an E on the circuit board.**
16. Insert all IC's into their respective sockets, observing correct orientation (pin 1 away from edge connectors). If a standard Digital Group CPU cabinet and the Phideck cabinet are being used, omit steps 17-19 and refer to Appendix L.
17. Wire the board into the microprocessor's I/O structure, as described below. Connect the Phideck by slipping the Molex connector supplied with the deck onto pins H - R of the controller's 36-pin socket. Orient the Molex connectors such that the orange wire is on pin R. This puts the deck into position Ø.
18. If deck 1 will also be used, connect its Molex connector similarly to the connector for deck Ø. Bend the pins out on the 36-pin socket and slip on the connector. Decks 2 and 3 must be rewired at the connector, since several of the necessary signal pins are common to all of the decks.
19. Connect the shielded pair from deck Ø to pins 1 and A. Connect the ground to pin 5 or E. If deck 1 is to be used, connect the shielded pair to pins 2 and B (reserve the connector's orientation) and rewire the ground pin into deck Ø's ground connector. For decks 2 and 3, a different method of connection must be employed, as no more Molex connectors will fit.
20. Remove the protective plastic shield from the digital head on the transport, if one has been supplied.

21. Proceed with the initial checkout of the board by following the steps under Section VII, DEBUG.

22. When the board seems to be working properly, perform the oscillator calibration and read amplifier gain calibration procedures under Section VI, CALIBRATION. Calibrate the motor speed only if it is absolutely necessary. The Cassette Storage System is now ready for use.

USING THE CONTROLLER IN A DIGITAL GROUP SYSTEM

The connection diagram in Figure 3.2 of the controller manual is used with the Digital Group Software packages. Refer to the wiring chart in Table 6.1 and to Appendix L, Phideck Connection Standards, for the proper connections to implement the wiring scheme in Figures 3.2. Appendix L covers cabling using a Digital Group CPU cabinet, Phideck cabinet and Phideck Interconnect cable. If the Phideck cabinet and Interconnect cable are not being used, make the connections in Table 6.1 and Detail 1 of Appendix L and follow the Deck Interface section for deck connections.

An optional, but highly recommended, stop switch may be wired to the controller. A normally open momentary push button which brings the manual stop pin ($\overline{B}$) to ground will stop all deck movement.

VI. CALIBRATION

OSCILLATOR CALIBRATION

To insure compatibility between decks and tapes among all users of this system, the data rate should be adjusted to meet the standard specifications. Before you proceed with the adjustment of R28, the controller must be placed in the record mode by issuing a record command from the computer. This disables the DC feedback path to pin 5 of IC9. Adjust R28 for a 112 KHz signal at pin 3 of IC9. In record mode, this will produce an 8 KHz signal on DCLK. This bit rate (8,000 bits/sec) will record 1,600 flux changes per inch at a tape speed of five inches per second. The data rate is then 6,400 baud when referenced to the data transfer rate between the computer and the controller.

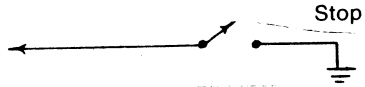
MOTOR SPEED CALIBRATION

The capstan motor on the Phideck is preadjusted to 5 ips at the factory. The following adjustment may be made periodically to keep the deck speed within tolerance. (Note: Side B of your tape has approximately one minute of a 4 KHz test signal recorded on it. This is equivalent to 1,600 FCPI.) Using the 4 KHz test signal recorded on the reverse side of the cassette supplied with your controller, monitor the tape signal in the read mode on IC13, pin 14. With a non-metallic screwdiver or alignment tool, adjust the tape speed through the hole on top of the capstan motor so that the frequency of the tape signal is 4 KHz.

Table 6.1

Wiring Chart

Phideck Board			**I/O Board (Ports Ø-3)**	
PIN #	DESCRIPTION	CONNECT TO	PIN #	DESCRIPTION
6	DO7		26	MSB
7	DO6		25	MSB-1
8	DO5 Data		24	MSB-2 Input
9	DO4 Output		23	MSB-3 Port 2
10	DO3 Lines		22	LSB+3
11	DO2		21	LSB+2
12	DO1		20	LSB+1
13	DOØ		19	LSB
14	Data Output Strobe		$\overline{R}$	MSB-3, Output Port 1
15	D17		$\overline{D}$	MSB
16	D16		$\overline{C}$	MSB-1 Output
17	D15		$\overline{B}$	MSB-2 Port 2
18	D14 Data		$\overline{A}$	MSB-3
19	D13 Input		Z	LSB+3
20	D12 Lines		Y	LSB+2
21	D11		X	LSB+1
22	D1Ø		W	LSB
23	Data Input Strobe		U	MSB, Output Port 1
L	*Not Busy		22	LSB+3
M	*Stop Status		21	LSB+2 Input
N	*Ready Port		20	LSB+1 Port 2
P	*Overrun/Underrun		19	LSB
R	Status Strobe		$\overline{S}$	MSB-2, Output Port 1
S	*Enable/Disable		$\overline{D}$	MSB
T	*Slow/Fast		$\overline{C}$	MSB-1
U	*FWD/BKWD Command		$\overline{B}$	MSB-2 Output
V	*Stop/Run Port		$\overline{A}$	MSB-3 Port 2
W	*RCD/READ		Z	LSB+3
X	*ERASE		Y	LSB+2
Y	*SEL2		X	LSB+1
$\overline{Z}$	*SEL2		W	LSB
$\overline{A}$	Command Strobe		T	MSB-1, Output Port 1
$\overline{B}$	$\overline{\text{Manstop}}$			



Momentary, Normally Open Switch

*These pins may actually be wired to the opposite pin on the Phideck Board connector (i.e., pin L to pin 10 on the Phideck Board).

READ AMPLIFIER GAIN CALIBRATION

First, record several minutes of test data onto a tape that you will be using. The Demo program on the Audio cassette supplied with the controller contains a routine for recording test data. (Once you have decided on a type of tape that gives you good results and that is readily available, you should not change tapes.) Now place the controller in read mode and read your tape. Monitor the signal at IC13, pin 1. If the amplitude is not within the limit shown in Figure 4.2, try different values of R18 until the amplitude is within limits. This adjustment is not critical and your controller will give good results even if your amplitude is not within the limits specified.

HEAD AZIMUTH ADJUSTMENT

Using the 4 KHz test signal recorded on the reverse side of the cassette supplied with your controller, monitor the tape signal on IC13, pin 1 with an oscilloscope. Adjust the Azimuth adjusting screw for maximum output. The azimuth adjusting screw is located on the left side of the head with a spring under it to maintain tension. After adjusting, seal the screw in place with insulating varnish or fingernail polish.

VII. DEBUG

Reread the software section to be certain the correct procedures are being executed. Insert controller card (do not connect Phideck yet) and turn power on. The Demo program on the Audio cassette supplied with the controller should be used to check out the basic functions of the controller. This will allow you to issue the basic motor commands and record a repetitive test data pattern. Do not use the test data options to test motor control functions. These are intended to check the read/record circuitry.

Issue input and output commands to the I/O ports and verify that the strobe signals are present when the command is issued. Also, verify that the data is being latched in the command and data latches correctly (IC33, 46, 47, and 28).

CONNECT THE PHIDECK AND PROCEED THROUGH THE FOLLOWING SECTIONS.

MOTOR CONTROL ELECTRONICS

Place an old cassette into the deck (if the motor control electronics is not working properly this test may destroy the tape). Issue a fast forward command and check tape movement (these commands are given in the Mechanical Considerations portion of this manual). Issue a fast reverse command and check tape movement. Remove cassette and issue a stop command. Both reel motors should turn in opposite directions. Reinsert the cassette and issue a record command. The head should engage the tape and the takeup reel should turn. Place your finger on the takeup reel motor pulley. The head should disengage within 1.5 seconds after stopping the motor. If any of the above tests fail, refer to the Theory of Operation for the motor drive and sense electronics and the motor control electronics and proceed to trace the problem.

HEAD SENSE AND BIT SYNCHRONIZING ELECTRONICS

Place controller in record mode and output data bytes to the controller every time READY comes true. You should see waveforms similar to those shown in Figure 4.1 at the outputs of the selected head driver (IC27 or IC28). Waveforms similar to these should also appear on the head of the selected drive.

The read amplifiers may be tested by using the tape you made in the previous paragraph, placing the deck in read mode after rewinding the tape, and looking for the waveforms given in Figure 4.2. If the voltage at IC13, pin 1 is clipping or not within the range shown, refer to Calibration for Adjustment. This adjustment is not critical and is probably not the cause of the controller malfunction.

The bit synchronizing electronics may be checked by verifying the timing diagram shown in Figure 4.3.

READ/WRITE ELECTRONICS

Test all of the clocking signals depicted in Figure 4.9. If a signal is not present or correct, trace back through the logic generating that signal. Make sure about 0.2 Volts of the tape head signal is present on record, and not on read. Check that RECORD reflects the selected state and RDY had a pulsing signal when recording or reading.

The basic clock, IC9, may be removed, and a bounceless switch (Figure 7.1) used to single step the system (14 clocks per data bit). If an oscilloscope is not available, an audio amplifier with the circuit in Figure 7.2 can be used to probe for clocks and data flow. For example, recording or reading in hex "5A" will sound like a 4 KHz square wave on pin 6 of IC5, and (on record) a 2 KHz square wave on pin 3 of IC4. (This signal is not present on erase and read.)

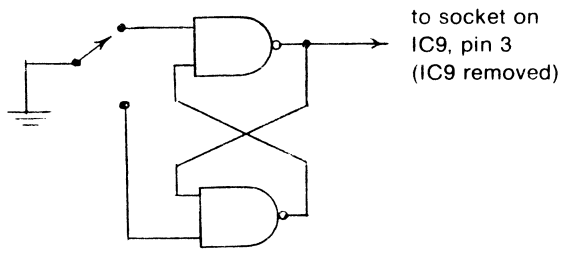


Figure 7.1 Single-step Clock

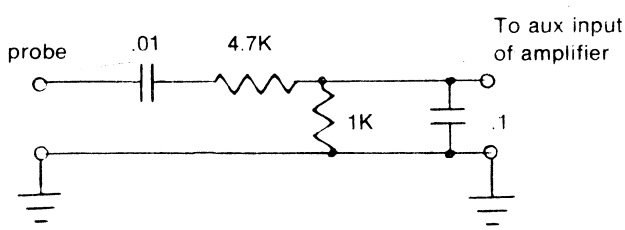


Figure 7.2 Digital to Audio Sensor

VIII. APPENDIX

A. Parts List

B. PROM Pattern

C. Connector Pinout

D. Transistor Orientation

E. Driver Software Description

F. Recording Format

G. Program Tape and Listings

H. Phideck Maintenance

I. Phideck Wiring

J. Phideck Connection Standards

K. Component Placement

L. Schematic

A. PARTS LIST

DESCRIPTION	QUANTITY	CIRCUIT REFERENCE
74S00	1	IC49
7400	8	IC1, 8, 10, 14, 16, 17, 25, 38
7402	1	IC15
7404	2	IC34, 40
7408	1	IC36
7410	2	IC19, 39
7411	1	IC18
7420	2	IC6, 22
7451	2	IC2, 24
7473	1	IC41
7474	6	IC3, 5, 21, 42, 50, 55
7475	4	IC33, 46, 47, 48
7486	1	IC26
7490	1	IC20
7493	2	IC7, 37
74107	1	IC4
74123	1	IC23
74125	3	IC27, 28, 45
74153	2	IC31, 32
74155	1	IC35
74173, 8551	2	IC43, 44
74195	1	IC30
74S188, 8223, 6330-1J	1	IC29
75451	4	IC51, 52, 53, 54
LM324	1	IC13
LM340T-8.0, uA7808	1	IC12
LM358	1	IC11
LM555	1	IC9
2N4403	4	T7, 8, 9, 10
2N5129	1	T12
2N5139	2	T6, 11
2N6109	4	T2, 3, 4, 5
2N6410, MJE2050	1	T1
MPF971	1	T13
1.5 ohm, ½W	1	R44
7.5 ohm, 1W	1	R46
18 ohm, 2W	1	R45
47 ohm	2	R53, 57
82 ohm	1	R27
220 ohm	1	R12
470 ohm	1	R48
510 ohm	1	R58
680 ohm	8	R32, 33, 34, 35, 36, 37, 38, 39
1K ohm	7	R6, 9, 20, 23, 26, 31, 55
1.2K ohm	4	R15, 16, 19, 30
2.2K ohm	2	R1, 29
4.7K ohm	2	R2, 49
5K ohm POT	1	R28
10K ohm	13	R7, 8, 10, 11, 14, 17, 21, 22, 24, 25, 43, 47, 54
22K ohm	3	R40, 41, 42
33K ohm	1	R50
39K ohm	2	R4, 5
47K ohm	1	R3
100K ohm	1	R13
150K ohm	2	R51, 52
220K ohm	1	R18
1 Meg ohm	1	R56

220 pfd mylar	1	C4
.0015 mfd mylar	1	C12
.0033 mfd mylar	1	C25
.005 mfd mylar	1	C3
.01 mfd disc	14	C5, 6, 7, 8, 9, 10, 11, 20, 21, 23, 26, 28, 29, 31
.1 mfd disc	2	C1, 24
1 mfd tantalum	9	C2, 15, 16, 17, 18, 19, 22, 30, 32
4.7 mfd tantalum	2	C27, 33
100 mfd electrolytic	2	C13, 14
1N4001	15	D1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15
1N4148	4	D16, 17, 18, 19
TO-220 heatsink, THM6072B	1	
4-40 screws	2	
4-40 nuts	2	
#4 lockwashers	2	
8-pin DIP sockets	6	
14-pin DIP sockets	36	
16-pin DIP sockets	12	
Dual 22-pin edge connectors	1	
Dual 36-pin edge connectors	1	
PC board	1	

B. PROM PATTERN

A4	A3	A2	A1	A0	B0	B1	B2	B3	B4	B5	B6	B7
0	0	0	0	0	1	1	0	1	1	1	0	0
0	0	0	0	1	1	1	1	1	0	0	0	0
0	0	0	1	0	1	0	1	0	1	0	0	0
0	0	0	1	1	1	0	1	1	0	0	1	0
0	0	1	0	0	1	1	0	1	1	1	0	0
0	0	1	0	1	1	0	0	1	0	0	0	1
0	0	1	1	0	1	0	1	0	1	0	0	0
0	0	1	1	1	1	0	1	1	1	0	1	0
0	1	0	0	0	1	1	1	0	1	1	1	0
0	1	0	0	1	0	1	0	1	1	0	1	0
0	1	0	1	0	0	1	1	0	1	1	0	0
0	1	0	1	1	0	1	1	1	1	1	1	0
0	1	1	0	0	1	1	1	0	1	1	1	0
0	1	1	0	1	0	1	0	1	1	0	1	0
0	1	1	1	0	0	1	1	0	1	1	0	0
0	1	1	1	1	0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	0	0	0	1	1	0
1	0	0	0	1	0	0	0	0	0	1	0	0
1	0	0	1	0	0	0	0	0	0	1	0	0
1	0	0	1	1	0	0	0	0	0	1	1	0
1	0	1	0	0	0	0	0	0	0	1	1	0
1	0	1	0	1	0	0	0	0	0	0	1	0
1	0	1	1	0	0	0	0	0	0	1	0	0
1	0	1	1	1	0	0	0	0	0	1	1	0
1	1	0	0	0	0	0	0	0	0	0	1	0
1	1	0	0	1	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	1	0	0	0
1	1	0	1	1	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1	0	0
1	1	1	0	1	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	1	0	0	0
1	1	1	1	1	0	0	0	1	0	0	1	0

C. CONNECTOR PINOUT

Top of Card - Component Side

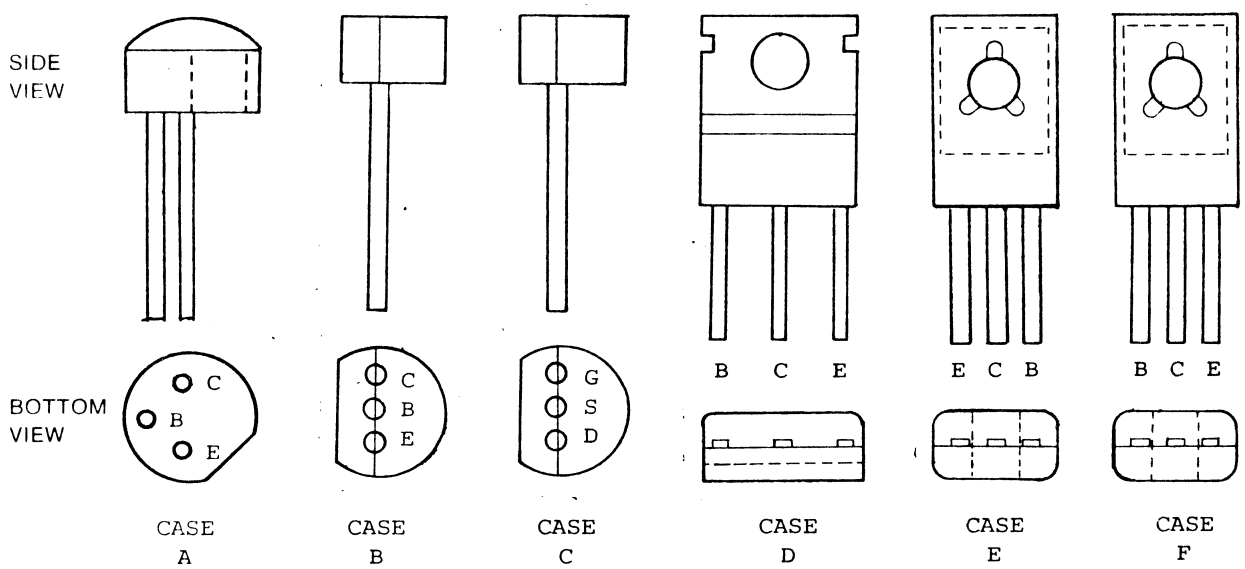
Pin No.	Description	
1	HDAØ	
2	HDA1	
3	HDA2	
4	HDA3	
5	HDGND	
6	DO7	
7	DO6	
8	DO5	Data
9	DO4	Output
10	DO3	Lines
11	DO2	
12	DO1	
13	DOØ	
14	Data Output Strobe	
15	DI7	
16	DI6	
17	DI5	
18	DI4	Data
19	DI3	Input
20	DI2	Lines
21	DI1	
22	DIØ	
23	Data Input Strobe	
24	+9V Out	
25	ENG3	
26	SUP3	
27	FWD3	
28	REV3	
29	ALLENGSW	
30	ALLENGSWGND	
31	CAPSUPPLY	
32	ALCAP	
33	ENG1	
34	SUP1	
35	FWD1	
36	REV1	

Bottom of Card - Circuit Side

Pin No.	Description	
A	HDBØ	
B	HDB1	
C	HDB2	
D	HDB3	
E	HDGND	
F	DATA READY IRQ	
H	n/c	
J	n/c	
K	n/c	
L	Not Busy	
M	Stop	Status
N	Ready	Port
P	Overrun/Underrun	
R	Status Strobe	
S	Enable/Disable	
T	Slow/Fast	
U	FWD/BKWD	Command
V	Stop/Run	Port
W	RCD/READ	
X	ERASE	
Y	SEL 2	
Z	SEL 1	
$\overline{A}$	Command Strobe	
$\overline{B}$	$\overline{\text{Manstop}}$	
$\overline{C}$	ENG2	
$\overline{D}$	SUP2	
$\overline{E}$	FWD2	
$\overline{F}$	REV2	
$\overline{H}$	ALLENGSW	
$\overline{J}$	ALLENGSWGND	
$\overline{K}$	CAPSUPPLY	
$\overline{L}$	ALCAP	
$\overline{M}$	ENGØ	
$\overline{N}$	SUPØ	
$\overline{P}$	FWDØ	
$\overline{R}$	REVØ	

Note: n/c = no connection
Pin 1 on 22-pin connector = +5V
Pin 2 on 22-pin connector = GND
Pin 22 on 22-pin connector = +12V

D. TRANSISTOR ORIENTATION



Transistor	Case
2N6109	D
2N5139	A or B
2N5129	A or B
2N4403	B
2N6410	F
MJE2050	E
MPF971	C

E. DRIVER SOFTWARE DESCRIPTION

The software supplied with the Digital Group Cassette Storage System contains deck control subroutines to allow the user to concentrate on applications. The READ and RECORD routines provide all error recovery during read, and data verification during record.

The software package consists of several major routines to aid the user in controlling the decks. These are the RECORD, CMDOUT, READ, and REWIND routines. There are numerous minor subroutines the user may invoke if he feels the need to control the deck on a more basic level.

The sample Z-80 program given below is a simple example of how to use the major routines. The sample program will read the tape on deck Ø and write the data on deck 1, one block at a time. This program will halt if an unrecoverable error occurs. The major routines are described in more detail following the example. This program will only copy tapes that have been recorded using the format detailed in Appendix F.

```
* SAMPLE PROGRAM TO COPY A TAPE
* ON DECK Ø TO A TAPE ON DECK 1
* ONE BLOCK AT A TIME
```

LABEL	OP	OPERAND	COMMENT
START	LD	A,Ø	SET DECK Ø
	LD	(DECK),A	
	CALL	REWIND	REWIND DECK Ø
	LD	A,1	SET DECK 1
	LD	(DECK),A	
	CALL	REWIND	REWIND DECK 1
	SUB	A	CLEAR REGISTER A
	LD	(TEMPID),A	INITIALIZE ID
REDBLK	IN	TAPEIN	WAIT FOR NOT BUSY
	AND	ØBH	BECAUSE THE DECK
	JP	Z,REDBLK	NUMBER IS CHANGING
	LD	A,Ø	SET DECK Ø
	LD	(DECK),A	
	LD	HL,BUFFER	SET UP POINTER
	LD	(POINTER),HL	
	LD	A,(TEMPID)	SET UP ID
	LD	(IDR),A	
	LD	E,Ø	SET READ MODE
	CALL	READ	READ BLOCK
	PUSH	AF	SAVE REGISTER A
	LD	C,FØH	STOP DECK
	CALL	CMDOUT	
	POP	AF	RESTORE REGISTER A
	CP	Ø	ERROR?
	JP	Z,WRTBLK	NO
	CP	2	BLOCK FOUND?
	RET	Z	NO, FINISHED
	HALT		HALT BECAUSE ERROR
WRTBLK	IN	TAPEIN	WAIT FOR NOT BUSY
	AND	ØBH	BECAUSE THE DECK
	JP	Z,WRTBLK	NUMBER IS CHANGING
	LD	A,1	SET DECK 1
	LD	(DECK),A	
	LD	HL,BUFFER	SET UP POINTER
	LD	(POINTW),HL	
	LD	A,(TEMPID)	SET UP ID
	LD	(IDW),A	
	INC	A	INCREMENT ID
	LD	(TEMPID),A	
	LD	A,B	SET UP COUNT
	CP	Ø	256?
	JP	Z,X256	YES
	LD	L,B	
	LD	H,Ø	
	JP	CALRCD	

```
X256        LD      H,1
            LD      L,Ø
CALRCD      CALL    RECORD          RECORD BLOCK
            CP      Ø               ERROR?
            JP      Z,REDBLK        NO, COPY NEXT BLOCK
            HALT                    HALT BECAUSE ERROR
TEMPID      DS      1
BUFFER      DS      256D
            END
```

The REWIND routine will stop the operating deck, select the specified deck, and rewind it. This routine returns to the calling routine after the selected deck has been rewound and readied for another command. Memory location "DECK" must contain the selected deck number (in binary) before the routine is called.

The RECORD routine will record data in the standard block format and then check the recorded data to verify that it was recorded without error. If an error is detected, that portion of the tape is erased and all the remaining data is re-recorded. This process is repeated until all data has been recorded successfully, or an unrecoverable error is detected.

As the user records data he must record blocks in sequence starting with IDW = Ø, 1, 2, etc. Numbers may not be skipped! After a series of blocks have been recorded, the user may re-record a block, but all old blocks following the new blocks may be lost. Although not absolutely necessary, it is recommended that tapes be erased with a bulk eraser or using the Phideck in erase mode to obtain maximum performance and prevent the controller software from becoming confused with the old data.

In order to use this routine properly, the input variables must be set up properly:

1. The deck number must be placed in memory location DECK.
2. The low order byte of the block ID must be placed in memory location IDW, and the high order byte must be placed in IDW+1.
3. The low order byte of the address of the first byte to be recorded is placed in memory location POINTW, and the high order byte is placed in POINTW+1.
4. The number of bytes to be recorded is placed in register pair H and L. A count of zero will cause the record routine to simply return without recording any data.

When the record routine returns control to the calling routine, the registers and memory are modified as follows:

1. All Registers are altered.
2. IDW returns the ID of the last block recorded plus one.
3. POINTW points one location greater than the last byte recorded.
4. The error code is returned in the A register and should be checked after every call to the RECORD routine. The error codes are:

    Ø - Record completed with no errors
    1 - CRC error in block ID-1
    2 - Block ID-1 not found
    3 - End of tape or jam

The READ routine will read one block and return to the calling routine. The deck is left running so the user must either read another block or issue a stop command to the deck directly (see the CMDOUT routine).

To use this routine the following variables must be set up properly:

1. The deck number is placed in memory location DECK.
2. Memory location IDR contains the low order byte of the ID of the block to be read. IDR+1 contains the high order byte.
3. Memory location POINTR contains the low order byte of the address of where the data is to be deposited. POINTR+1 contains the high order byte.
4. Register E contains the mode. Ø indicates that the data block is to be read into memory starting at the location specified by POINTR. 1 indicates that the data block is to be checked for errors only (in this mode POINTR is not used).
5. RETRYS (Register D) should be initialized only if the ALTRD or ALTRD2 entry points are used. It is automatically initialized to 10 if the READ entry point is used. The user should normally use the READ entry point.

When the read routine returns control to the calling routine, the registers and memory are modified as follows:

1. Registers A, B, C, D, H, and L are modified.
2. COUNT (Register B) contains the number of bytes contained in the block:

   Ø = 256 bytes
   1 = 1 byte
   2 = 2 bytes
   255 = 255 bytes

3. ERROR (Register A) contains the error code after a read operation has been completed. The error codes are:

   Ø - No errors
   1 - Unrecoverable data error
   2 - Unable to find block specified by ID
   3 - End of tape or jam

The CMDOUT routine is used to issue commands to the transport. Memory location DECK must contain the number of the deck that is referenced by command. Register C must contain the command to be issued to the deck. The valid commands are:

COMMAND	VALUE IN REGISTER C	
STOP	1 1 1 1	0 0 0 0
FAST FORWARD	1 0 1 0	0 0 0 0
FAST REVERSE	1 0 0 0	0 0 0 0
READ	1 1 1 0	0 0 0 0
RECORD	1 1 1 0	1 0 0 0
ERASE	1 1 1 0	1 1 0 0
STANDBY	0 1 1 1	0 0 0 0

F. RECORDING FORMAT

This appendix shows the block format as it is recorded on the tape by the driver software and controller. Each byte recorded on the tape consists of 10 bits or flux changes (see hardware description).

DESCRIPTION	BYTES RECORDED
75 one bits	7.5
SYNC character	.5
ID high	1.
ID low	1.
COUNT	1.
CRC 1	1.
CRC 2	1.
DATA	1. to 256
CRC 1	1.
CRC 2	1.
TOTALS*	16 to 271

*The record routine will erase to an equivalent of 271 bytes for short blocks so that all blocks will be the same size.

G. PROGRAM TAPE AND LISTINGS

The tape supplied with the program listing is an AUDIO CASSETTE recorded at 1100 Baud in Suding format. This **WILL NOT** load from the Phideck.

The program tape contains the following programs in the order given in a 64 character version then a 32 character version for a total of eight tone bursts.

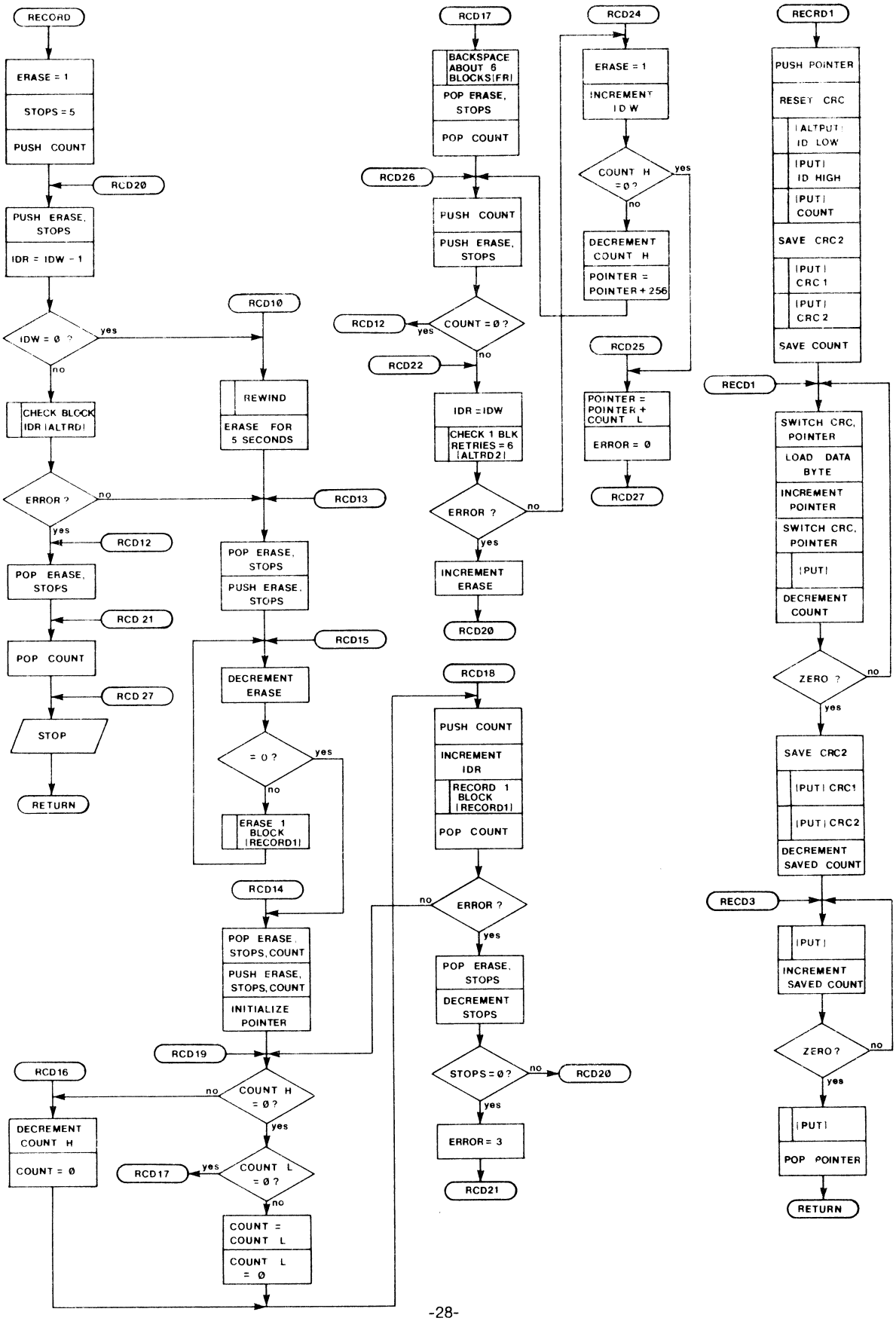
1. Phideck Demo for Z-80
2. Z-80 Ops System
3. Phideck Demo for 8080
4. 8080 Ops System

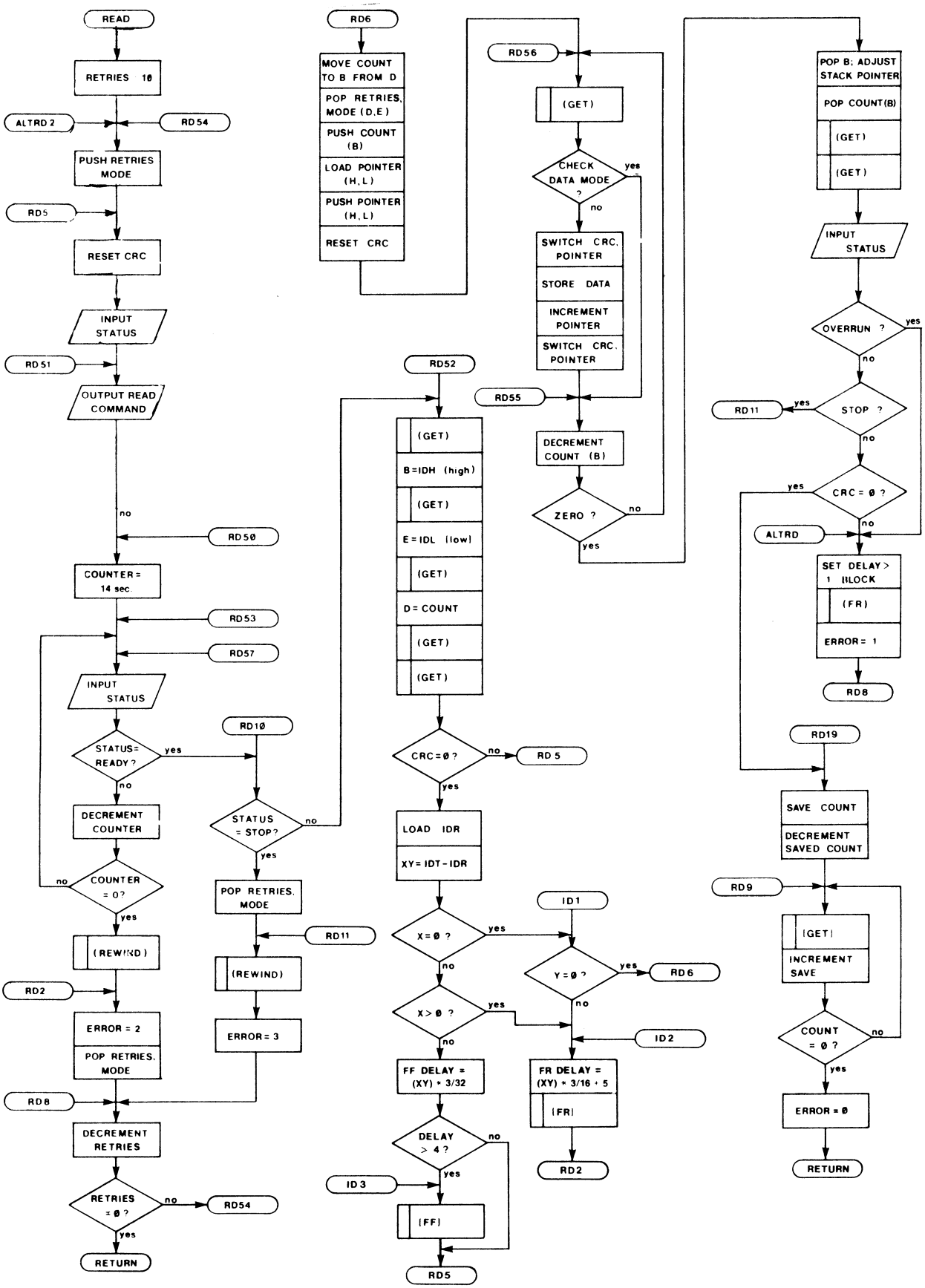
Each program includes the Phideck driver routines in the program listing in locations 0900H thru 0B9DH. The Demo Software is included as an aid in testing the controller.

Note: Listings are provided only for the Z-80 Software, however, the 8080 Driver Software object code is exactly the same as for the Z-80.

USING PHIDECK DEMO SOFTWARE

1. Programs are loaded via audio cassette.
2. At completion of a successful load a listing of Phideck commands will be displayed.
3. In addition to the displayed options, there are three possible options - "R", "S", and "P".
4. "R" will return control to the Operating System.
5. "S" will display memory in either hex or octal depending upon last option (hex or octal) chosen by the user.
6. "P" will allow user to program as in the Operating System in either hex or octal depending upon last method chosen.
7. Reset will return control to Phideck Ops.
8. "P", "R", and "S" will operate when in Storage Dump, Program, or Phideck Ops.
9. Phideck option "#" allows the user to select any of 4 decks (0-3) by pressing shift # then desired deck number. To return to Phideck Ops press Y. The selected deck number will be displayed in the options listing upon return.
10. Phideck option "0" will copy a tape from deck 0 to deck 1. This is not intended as an efficient method of duplicating tapes, only as a demostration of Phideck routines. Only tapes recorded in the format detailed in Appendix F may be copied using this option.
11. Page0DH is being used as a 256 byte buffer in the Copy Tape option.
12. Phideck option "1" will erase a tape on the selected deck.
13. Phideck option "2" will fast reverse the selected deck.
14. Phideck option "3" will fast forward the selected deck.
15. Phideck option "4" will place all decks in standby. The capstan motors will be turned off.
16. Phideck option "5" will stop the selected deck.
17. Phideck option "6" will issue a read command to the selected deck. This **will not** read data from a tape.
18. Phideck option "7" will issue a record command to the selected deck. This **will not** record data on a tape.
19. Phideck option "8" will record 256 byte blocks of data in a fixed pattern. The test data recorded is not formatted in accordance with Appendix F.
20. Phideck option "9" will read byte blocks of data from a tape in a fixed pattern. An "e" will be displayed on the monitor for blocks in error and a "g" for good blocks.


RECORD
ERASE = 1
STOPS = 5
PUSH COUNT
RCD20
PUSH ERASE, STOPS
IDR = IDW - 1
IDW = Ø ?
yes
no
CHECK BLOCK IDR (ALTRD)
ERROR ?
no
yes
RCD12
POP ERASE, STOPS
RCD 21
POP COUNT
RCD 27
STOP
RETURN
RCD10
REWIND
ERASE FOR 5 SECONDS
RCD13
POP ERASE, STOPS
PUSH ERASE, STOPS
RCD15
DECREMENT ERASE
= Ø ?
yes
no
ERASE 1 BLOCK (RECORD1)
RCD14
POP ERASE, STOPS, COUNT
PUSH ERASE, STOPS, COUNT
INITIALIZE POINTER
RCD19
RCD16
no
COUNT H = Ø ?
yes
DECREMENT COUNT H
COUNT = Ø
RCD17
yes
COUNT L = Ø ?
no
COUNT = COUNT L
COUNT L = Ø
RCD17
BACKSPACE ABOUT 6 BLOCKS (FR)
POP ERASE, STOPS
POP COUNT
RCD26
PUSH COUNT
PUSH ERASE, STOPS
RCD12
yes
COUNT = Ø ?
no
RCD22
IDR = IDW
CHECK 1 BLK RETRIES = 6 (ALTRD2)
ERROR ?
no
yes
INCREMENT ERASE
RCD20
RCD18
PUSH COUNT
INCREMENT IDR
RECORD 1 BLOCK (RECORD1)
POP COUNT
no
ERROR ?
yes
POP ERASE, STOPS
DECREMENT STOPS
STOPS = Ø?
no
RCD20
yes
ERROR = 3
RCD21
RCD24
ERASE = 1
INCREMENT IDW
COUNT H = Ø ?
yes
no
DECREMENT COUNT H
POINTER = POINTER + 256
RCD25
POINTER = POINTER + COUNT L
ERROR = Ø
RCD27
RECRD1
PUSH POINTER
RESET CRC
(ALTPUT) ID LOW
(PUT) ID HIGH
(PUT) COUNT
SAVE CRC2
(PUT) CRC 1
(PUT) CRC 2
SAVE COUNT
RECD1
SWITCH CRC, POINTER
LOAD DATA BYTE
INCREMENT POINTER
SWITCH CRC, POINTER
(PUT)
DECREMENT COUNT
ZERO ?
no
yes
SAVE CRC2
(PUT) CRC1
(PUT) CRC2
DECREMENT SAVED COUNT
RECD3
(PUT)
INCREMENT SAVED COUNT
ZERO ?
no
yes
(PUT)
POP POINTER
RETURN


READ
RETRIES 10
ALTRD 2
RD54
PUSH RETRIES MODE
RD5
RESET CRC
INPUT STATUS
RD51
OUTPUT READ COMMAND
no
RD50
COUNTER = 14 sec
RD53
RD57
INPUT STATUS
STATUS = READY ?
yes
no
RD10
DECREMENT COUNTER
COUNTER = 0 ?
no
yes
(REWIND)
RD2
ERROR = 2
POP RETRIES, MODE
RD8
STATUS = STOP ?
no
yes
POP RETRIES, MODE
RD11
(REWIND)
ERROR = 3
DECREMENT RETRIES
RETRIES = 0 ?
no
RD54
yes
RETURN
RD6
MOVE COUNT TO B FROM D
POP RETRIES, MODE (D,E)
PUSH COUNT (B)
LOAD POINTER (H,L)
PUSH POINTER (H,L)
RESET CRC
RD52
(GET)
B=IDH (high)
(GET)
E=IDL (low)
(GET)
D=COUNT
(GET)
(GET)
CRC=0 ?
no
RD5
yes
LOAD IDR
XY=IDT-IDR
X=0 ?
yes
ID1
no
X>0 ?
yes
no
FF DELAY = (XY) * 3/32
DELAY > 4 ?
no
ID3
yes
(FF)
RD5
Y=0 ?
yes
RD6
no
ID2
FR DELAY = (XY) * 3/16 + 5
(FR)
RD2
RD56
(GET)
CHECK DATA MODE ?
yes
no
SWITCH CRC. POINTER
STORE DATA
INCREMENT POINTER
SWITCH CRC. POINTER
RD55
DECREMENT COUNT (B)
ZERO ?
no
yes
POP B; ADJUST STACK POINTER
POP COUNT(B)
(GET)
(GET)
INPUT STATUS
OVERRUN ?
yes
no
RD11
yes
STOP ?
no
yes
CRC = 0 ?
no
ALTRD
no
SET DELAY > 1 BLOCK
(FR)
ERROR = 1
RD8
RD19
SAVE COUNT
DECREMENT SAVED COUNT
RD9
(GET)
INCREMENT SAVE
COUNT = 0 ?
no
yes
ERROR = 0
RETURN

```
LOC  OBJ                    LABEL   OP    OPERAND COMMENTS
0900                        0250        ST    0900H
0900                        0260  * RECORD (UNTIL COUNT EXHAUSTED)
0900                        0270  * DECK IS STOPPED AFTER RETURN
0900                        0280  * INPUT:
0900                        0290  *       DECK - DECK NUMBER LOCATED IN MEMORY
0900                        0300  *       POINTW - LOCATED IN MEMORY
0900                        0310  *                  (FIRST DATA BYTE)
0900                        0320  *       IDW - LOCATED IN MEMORY (FIRST BLOCK)
0900                        0330  *       COUNT - REGISTER H,L
0900                        0340  * OUTPUT:
0900                        0350  *       POINTW - LOCATED IN MEMORY
0900                        0360  *                  (LAST DATA BYTE + 1)
0900                        0370  *       ERROR - REGISTER A
0900                        0380  *                0 - NO ERRORS
0900                        0390  *                1 - CRC ERROR IN BLOCK
0900                        0400  *                    IDW - 1
0900                        0410  *                2 - BLOCK IDW-1 NOT FOUND
0900                        0420  *                3 - TAPE END OR JAM
0900                        0430  *       IDW - LOCATED IN MEMORY
0900                        0440  *             (LAST BLOCK + 1)
0900                        0450  *       ALTERED
0900                        0460  *             REGISTERS - A,F,C,I,E,B,L,IDR,POINTR
0900 1E 01                  0470  RECORD  LD    D,1D    ERASE=1
0902 1E 05                  0480        LD    E,5D    STOPS=5
0904 F5                     0490        PUSH  HL      COUNT
0905 D5                     0500  RCD20   PUSH  DE      ERASE, STOPS
0906 2A F5 0A               0510        LD    HL,(IDW)
0909 2B                     0520        DEC   HL      IDR=IDW -1
090A 22 F1 0A               0530        LD    (IDR),HL
090D 23                     0540        INC   HL
090E 7D                     0550        LD    A,L     IDW=0?
090F B4                     0560        OR    H
0910 CA 29 09               0570        JP    Z,RCD10 YES
0913 16 0F                  0580        LD    D,11D   RETRIES = 10
0915 1E 01                  0590        LD    E,1D    CHECK MODE
0917 CD 7F 0B               0600        CALL  ALTRD
091A 3C                     0610        INC   A       ERROR?
091B 3D                     0620        DEC   A
091C CA 3F 09               0630        JP    Z,RCD13 NO
091F D1                     0640  RCD12   POP   DE      ERASE, STOPS
0920 E1                     0650  RCD21   POP   HL      COUNT
0921 0E 90                  0660  RCD27   LD    C,90H   STOP
0923 47                     0670        LD    B,A     SAVE ERROR
0924 CD 93 0A               0680        CALL  CMDOUT
0927 78                     0690        LD    A,B     RESTORE ERROR
0928 C9                     0700        RET
0929 CD 47 0A               0710  RCD10   CALL  REWIND
092C 0E EC                  0720        LD    C,0ECH  ERASE
092E CD 93 0A               0730        CALL  CMDOUT
0931 3E 32                  0740        LD    A,50D   5 SECONDS
0933 CD 81 0A               0750        CALL  DELAY
0936 D1                     0760  RCD13   POP   DE      ERASE, STOPS
0937 D5                     0770        PUSH  DE
0938 15                     0780  RCD15   DEC   D       ERASE (ERASE - 1) BLOCKS
0939 CA 49 09               0790        JP    Z,RCD14
093C 0E EC                  0800        LD    C,0ECH  ERASE
```

```
093E CD 9E 0A      0650          CALL CMDOUT
0941 E5            0660          PUSH DE
0942 CD DA 09      0670          CALL RECRD1
0945 E1            0680          POP  DE
0946 C3 3E 09      0690          JP   RCD15
0949 E1            0700 RCD14    POP  HL       ERASE, STOPS
094A D1            0710          POP  DE       COUNT
094B E5            0720          PUSH DE
094C E5            0730          PUSH HL
094D 2A F7 0A      0740          LD   HL,(POINTW) POINTER
0950 15            0750 RCD19    DEC  D        COUNT HIGH =0?
0951 14            0760          INC  D
0952 C2 D4 09      0770          JP   NZ,RCD16 NO
0955 1D            0780          DEC  E
0956 1C            0790          INC  E
0957 CA 81 09      0800          JP   Z,RCD17 YES
095A 43            0810          LD   B,E      COUNT = COUNTL
095B 16 00         0820          LD   E,0D     COUNTL =0
095D D5            0830 RCD18    PUSH DE       SAVE COUNT
095E EB            0840          EX   DE,HL
095F 2A F1 0A      0850          LD   HL,(IDR)
0962 23            0860          INC  HL
0963 22 B1 0A      0870          LD   (IDR),HL
0966 EB            0880          EX   DE,HL
0967 0E E8         0890          LD   C,0E8H RECORD
0969 CD 9B 0A      0900          CALL CMDOUT
096C CD DA 09      0910          CALL RECRD1
096F DB 02         0920          IN   TAPEIN ERROR?
0971 E6 0D         0930          ANL  0DH
0973 D1            0940          POP  DE       GET COUNT
0974 CA 50 09      0950          JP   Z,RCD19 NO
0977 E1            0960          POP  DE       DECREMENT STOPS
0978 1D            0970          DEC  E        0?
0979 C2 05 09      0980          JP   NZ,RCD20 NO
097C 3E 03         0990          LD   A,3D     ERROR=3
097E C3 20 09      1000          JP   RCD21
0981 3E 03         1010 RCD17    LD   A,3D     APPROXIMATELY 6 BLOCKS
0983 CD 6E 0A      1020          CALL FR
0986 E1            1030          POP  HL       ERASE, STOPS
0987 D1            1040          POP  DE       COUNT
0988 D5            1050 RCD26    PUSH DE
0989 E5            1060          PUSH HL
098A 97            1070          SUB  A        COUNT=0?
098B B2            1080          ADD  D
098C C2 93 09      1090          JP   NZ,RCD22 NO
098F B3            1100          ADD  E
0990 CA 1F 09      1110          JP   Z,RCD12 YES
0993 2A B5 0A      1120 RCD22    LD   HL,(IDW)
0996 22 B1 0A      1130          LD   (IDR),HL
0999 16 06         1140          LD   D,6D     RETRIES = 6
099B 1E 01         1150          LD   E,1D     CHECK MODE
099D CD FF 0A      1160          CALL ALTRD2
09A0 3C            1170          INC  A        ERROR?
09A1 3D            1180          DEC  A
09A2 D1            1190          POP  DE
09A3 CA AA 09      1200          JP   Z,RCD24 NO
09A6 14            1210          INC  D        INCREMENT ERASE
09A7 C3 25 09      1220          JP   RCD20
09AA 16 01         1230 RCD24    LD   D,1D     ERASE=1
09AC 2A B5 0A      1240          LD   HL,(IDW) INCREMENT IDW
09AF 23            1250          INC  HL
```

```
09B0 22 B5 0A      1260          LD    (IDW),HL
09B3 EB            1270          EX    DE,HL
09B4 D1            1280          POP   DE
09B5 14            1290          INC   D       COUNTH =0?
09B6 15            1300          DEC   D
09B7 CA C7 09      1310          JP    Z,RCD25 YES
09BA 15            1320          DEC   D       DECREMENT COUNTH
09BB E5            1330          PUSH  HL
09BC 2A B7 0A      1340          LD    HL,(POINTW)
09BF 24            1350          INC   H
09C0 22 B7 0A      1360          LD    (PCINTW),HL
09C3 E1            1370          POP   HL
09C4 C3 88 09      1380          JP    RCD26
09C7 2A B7 0A      1390 RCD25    LD    HL,(POINTW) ADD COUNTL TO POINTER
09CA 16 00         1400          LD    D,0D
09CC 19            1410          ADD   HL,DE
09CD 22 B7 0A      1420          LD    (PCINTW),HL
09D0 97            1430          SUB   A       ERROR =0
09D1 C3 21 09      1440          JP    RCD27
09D4 15            1450 RCD16    DEC   D       DECREMENT COUNTH
09D5 06 00         1460          LD    B,0D    COUNT=0
09D7 C3 5D 09      1470          JP    RCD18
09DA               1480 * RECRD1 (RECORD ONE BLOCK)
09DA               1490 *          RECORD OR ERASE COMMANT MUST BE ISSUED
09DA               1500 *            BEFORE CALLING.
09DA               1510 *          UNDERRUN AND STOP SHOULD BE CHECKED
09DA               1520 *            AFTER RETURN.
09DA               1530 *
09DA               1540 *          INPUTS:
09DA               1550 *            DECK - DECK NUMBER LOCATED
09DA               1560 *                   IN MEMORY
09DA               1570 *            ID - REGISTER D,E
09DA               1580 *            COUNT - REGISTER B
09DA               1590 *                    (01=1 BYTE, 00=256 BYTES)
09DA               1600 *            POINTER - REGISTER H,L
09DA               1610 *                      (FIRST DATA BYTE)
09DA               1620 *          OUTPUT:
09DA               1630 *            POINTER - REGISTER H,L
09DA               1640 *            (LAST DATA BYTE + 1)
09DA               1650 *          ALTERED
09DA               1660 *            REGISTERS - A,B,C,D,E,H,L
09DA E5            1670 RECRD1   PUSH HL      PUSH POINTER
09DB 21 00 00      1680          LD    HL,0D   RESET CRC
09DE 4A            1690          LD    C,D,    ID HIGH
09DF CD 49 0A      1700          CALL  ALTPUT
09E2 4B            1710          LD    C,E     ID LOW
09E3 CD 42 0A      1720          CALL  PUT
09E6 48            1730          LD    C,B     COUNT
09E7 CD 42 0A      1740          CALL  PUT
09EA 54            1750          LD    D,H     SAVE CRC2
09EB 4D            1760          LD    C,L     CRC1
09EC CD 42 0A      1770          CALL  PUT
09EF 4A            1780          LD    C,D     CRC2
09F0 CD 42 0A      1790          CALL  PUT
09F3 58            1800          LD    E,B     SAVE COUNT
09F4 E3            1810 RECD1    EX    (SP),HL SWITCH CRC, POINTER
09F5 4E            1820          LD    C,(HL) LOAD DATA
09F6 23            1830          INC   HL      INCREMENT POINTER
09F7 E3            1840          EX    (SP),HL SWITCH CRC,POINTER
09F8 CD 42 0A      1850          CALL  PUT
09FB 05            1860          DEC   B       DECREMENT COUNT
```

```
09FC C2 F4 09      1870          JP   NZ,RECD1 NOT ZERO
09FF 54            1880          LD   D,H     SAVE CRC2
0A00 4D            1890          LD   C,L     CRC1
0A01 CD 42 0A      1900          CALL PUT
0A04 4A            1910          LD   C,D     CRC2
0A05 CD 42 0A      1920          CALL PUT
0A08 1D            1930          DEC  E       DECREMENT SAVED COUNT
0A09 CD 42 0A      1940 RECD3    CALL PUT
0A0C 1C            1950          INC  E       INCREMENT SAVED COUNT
0A0D C2 09 0A      1960          JP   NZ,RECD3 NOT ZERO
0A10 CD 42 0A      1970          CALL PUT
0A13 E1            1980          POP  HL      POP POINTER
0A14 C9            1990          RET
0A15               2000 *         GET
0A15               2010 *         CRC IN H,L
0A15               2020 *         DATA RETURNED IN C
0A15               2030 *         A,C,H,L ALTERED
0A15 DB 02         2040 GET      IN   TAPEIN STATUS
0A17 E6 0F         2050          AND  0FH
0A19 CA 15 0A      2060          JP   Z,GET
0A1C CD 8F 0A      2070          CALL DIN
0A1F D5            2080 CRC      PUSH DE
0A20 79            2090          LD   A,C
0A21 AD            2100          XOR  L
0A22 6F            2110          LD   L,A
0A23 1E 07         2120          LD   E,7D    7 TIMES
0A25 17            2130 CRCA     RLA  A
0A26 AD            2140          XOR  L
0A27 1D            2150          DEC  E
0A28 C2 25 0A      2160          JP   NZ,CRCA DONE?
0A2B 6F            2170          LD   L,A     YES
0A2C 0F            2180          RRCA A
0A2D 0F            2190          RRCA A
0A2E 5F            2200          LD   E,A     SAVE 1
0A2F E6 C0         2210          AND  0C0H
0A31 AC            2220          XOR  H
0A32 57            2230          LD   D,A     SAVE 2
0A33 7B            2240          LD   A,E     RESTORE 1
0A34 E6 3F         2250          AND  3FH
0A36 AD            2260          XOR  L
0A37 67            2270          LD   H,A     CRC HIGH DONE
0A38 17            2280          RLA  A       TEST BIT 7
0A39 7A            2290          LD   A,D     RESTORE 2
0A3A D2 3F 0A      2300          JP   NC,CRCFIN BIT 7 WAS 1?
0A3D EE 01         2310          XOR  1D      YES
0A3F 6F            2320 CRCFIN   LD   L,A     CRC LOW DONE
0A40 D1            2330          POP  DE
0A41 C9            2340          RET
0A42               2350 *         PUT
0A42               2360 *         DATA IN REGISTER C
0A42               2370 *         CRC IN H,L
0A42               2380 *         A,H,L ALTERED
0A42 DB 02         2390 PUT      IN   TAPEIN STATUS
0A44 E6 0F         2400          AND  0FH
0A46 CA 42 0A      2410          JP   Z,PUT
0A49 CD A8 0A      2420 ALTPUT   CALL DOUT
0A4C C3 1F 0A      2430          JP   CRC
0A4F               2440 *         REWIND
0A4F               2450 *         REGISTER A,C ALTERED
0A4F               2460 *         THIS ROUTINE WILL GUARANTEE
0A4F               2470 *         DECK SELECTION
```

```
0A4F 0E 90        2480 REWIND LD   C,90H  STOP
0A51 CD 9B 0A     2490        CALL CMDOUT
0A54 DB 02        2500 REWB   IN   TAPEIN
0A56 E6 08        2510        AND  08H
0A58 CA 54 0A     2520        JP   Z,REWB
0A5B 0E 80        2530        LD   C,90H FR
0A5D CD 9B 0A     2540        CALL CMDOUT
0A60 DB 02        2550 REWA   IN   TAPEIN
0A62 E6 08        2560        AND  8D
0A64 CA 60 0A     2570        JP   Z,REWA
0A67 C9           2580        RET
0A68              2590 *      FAST REVERSE, FAST FORWARD
0A68              2600 *      REGISTER A CONTAINS MULTIPLE
0A68              2610 *      OF 100 MILLI-SECONDS DELAY
0A68              2620 *      REGISTER A ALTERED
0A68 C5           2630 FR     PUSH BC
0A69 F5           2640        PUSH AF
0A6A 0E 80        2650        LD   C,80H
0A6C CD 9B 0A     2660 FRA    CALL CMDOUT
0A6F F1           2670        POP  AF
0A70 CD 81 0A     2680        CALL DELAY
0A73 0E 92        2690        LD   C,90H
0A75 C3 C2 0A     2700        JP   STOP
0A78 00           2710        NOP
0A79 00           2720        NOP
0A7A C5           2730 FF     PUSH BC
0A7B F5           2740        PUSH AF
0A7C 0E A0        2750        LD   C,0A0H
0A7E C3 6C 0A     2760        JP   FRA
0A81              2770 *      DELAY MULTIPLE OF 100 MS IN REGISTER A
0A81              2780 *      REGISTERS A,B,C ALTERED
0A81 01 B4 29     2790 DELAY  LD   BC,29B4H
0A84 0B           2800 D1     DEC  BC
0A85 04           2810        INC  B
0A86 05           2820        DEC  B
0A87 C2 84 0A     2830        JP   NZ,D1
0A8A 3D           2840        DEC  A
0A8B C2 81 0A     2850        JP   NZ,DELAY
0A8E C9           2860        RET
0A8F              2870 *      INPUT DATA BYTE (DATA RETURNED IN C)
0A8F              2880 *      REGISTER A IS ALTERED
0A8F 3E EF        2890 DIN    LD   A,0EFH
0A91 D3 01        2900        OUT  STROBE
0A93 DB 02        2910        IN   TAPEIN
0A95 4F           2920        LD   C,A
0A96 3E DF        2930 DINA   LD   A,0DFH
0A98 D3 01        2940        OUT  STROBE
0A9A C9           2950        RET
0A9B              2960 *      OUTPUT COMMAND (DATA IN REGISTER C)
0A9B              2970 *      DECK IS OR'D WITH DATA
0A9B              2980 *      REGISTER A IS ALTERED
0A9B 3A F0 0A     2990 CMDOUT LD   A,(DECK)
0A9E B1           3000        OR   C
0A9F D3 02        3010        OUT  TAPOUT
0AA1 3E 9F        3020        LD   A,9FH
0AA3 D3 01        3030 CMDA   OUT  STROBE
0AA5 C3 96 0A     3040        JP   DINA
0AA8              3050 *      OUTPUT DATA (DATA IN REGISTER C)
0AA8              3060 *      REGISTER A IS ALTERED
0AA8 79           3070 DOUT   LD   A,C
0AA9 D3 02        3080        OUT  TAPOUT
```

```
0AAB 3E 5F          3090          LD   A,5FH
0AAD C3 A3 0A       3100          JP   CMDA
0AB0                3110 *        VARIABLE DATA AREA
0AB0                3120 DECK     DS   1D      DECK NUMBER TO BE USED
0AB1                3130 IDR      DS   2D      READ ID
0AB3                3140 POINTR   DS   2D      READ POINTER
0AB5                3150 IDW      DS   2D      WRITE ID
0AB7                3160 POINTW   DS   2D      WRITE POINTER
0AB9                3170 *        READ ONE BLOCK
0AB9                3180 *          DECK REMAINS RUNNING AFTER RETURN
0AB9                3190 *        INPUT:
0AB9                3200 *          DECK - DECK NUMBER LOCATED IN MEMORY
0AB9                3210 *          POINTR - LOCATED IN MEMORY
0AB9                3220 *                   (FIRST BYTE)
0AB9                3230 *          IDR - LOCATED IN MEMORY
0AB9                3240 *          RETRYS - REGISTER D
0AB9                3250 *                   (ALTRD ONLY)
0AB9                3260 *          MODE - REGISTER E
0AB9                3270 *                 0=READ
0AB9                3280 *                 1=CHECK
0AB9                3290 *          CUTPUT:
0AB9                3300 *            DECK, POINTER, IDR UNCHANGED
0AB9                3310 *            REGISTER - A,B,C,D,H,L ALTERED
0AB9                3320 *            COUNT - REGISTER B
0AB9                3330 *                    01=1 BYTE
0AB9                3340 *                    00=256 BYTES
0AB9                3350 *            ERROR - REGISTER A
0AB9                3360 *                    0=NO ERRORS
0AB9                3370 *                    1=CRC ERROR
0AB9                3380 *                    2=BLOCK NO1 FOUND
0AB9                3390 *                    3=END OF TAPE OR JAM
0AB9                3400 *            ENTRY POINTS:
0AB9                3410 *              READ - NORMAL ENTRY
0AB9                3420 *              ALTRD - DECK WILL BACKSPACE
0AB9                3430 *                      FIRST, USER MUST SUPPLY RETRIES
0AB9                3440 *              ALTRD2 - NORMAL, EXCEPT USER MUST
0AB9                3450 *                       SUPPLY RETRIES.
0AB9 16 0A          3460 READ     LD   D,10D  RETRIES
0ABB D5             3470 RD54     PUSH DE     RETRIES, MODE
0ABC                3480 ALTRD2   EQU  RD54
0ABC 21 00 00       3490 RD5      LD   HL,0D  RESET CRC
0ABF C3 D2 0A       3500          JP   RD51
0AC2 CD 9B 0A       3510 STOP     CALL CMDOUT STOP ROUTINE
0AC5 3E 01          3520          LD   A,1    .1 SECOND
0AC7 CD 81 0A       3530          CALL DELAY
0ACA C1             3540          POP  BC
0ACB C9             3550          RET
0ACC CD 68 0A       3560 FRCOR    CALL FR     FAST REVERSE CORRECTION
0ACF C3 EE 0A       3570          JP   RD2
0AD2 0E E0          3580 RD51     LD   C,0E0H READ
0AD4 CD 9B 0A       3590          CALL CMDOUT
0AD7 06 48          3600 RD50     LD   B,48H  14 SECONDS
0AD9 50             3610 RD57     LD   D,B
0ADA DB 02          3620 RD53     IN   TAPEIN STATUS
0ADC E6 0F          3630          AND  0FH    READY?
0ADE C2 90 0B       3640          JP   NZ,RD10 YES
0AE1 1B             3650          DEC  DE
0AE2 14             3660          INC  D
0AE3 15             3670          DEC  D
0AE4 C2 DA 0A       3680          JP   NZ,RD53
0AE7 05             3690          DEC  B
```

```
0AE8 C2 D9 0A     3700          JP   NZ,RD57
0AEB CD 4F 0A     3710          CALL REWIND
0AEE 3E 0?        3720 RD2      LD   A,2D     ERROR=2
0AF0 D1           3730          POP  DE       RETRIES, MODE
0AF1 15           3740 RD8      DEC  D
0AF2 C2 BB 0A     3750          JP   NZ,RD54
0AF5 C9           3760          RET
0AF6 CD 15 0A     3770 RD52     CALL GET      IDH
0AF9 41           3780          LD   B,C
0AFA CD 15 0A     3790          CALL GET      IDL
0AFD 59           3800          LD   E,C
0AFE CD 15 0A     3810          CALL GET      COUNT
0B01 51           3820          LD   D,C
0B02 CD 15 0A     3830          CALL GET      CRC1
0B05 CD 15 0A     3840          CALL GET      CRC2
0B08 97           3850          SUB  A        CRC=0?
0B09 84           3860          ADD  H
0B0A C2 BC 0A     3870          JP   NZ,RD5   NO
0B0D 85           3880          ADD  L
0B0E C2 BC 0A     3890          JP   NZ,RD5   NO
0B11              3900 *        COMPUTE        BE  TAPEID
0B11              3910 *                       -HL  IDR
0B11              3920 *                       =XY
0B11 7B           3930          LD   A,E
0B12 2A B1 0A     3940          LD   HL,(IDR)
0B15 95           3950          SUB  L
0B16 5F           3960          LD   E,A      REGISTER E CONTAINS Y
0B17 6F           3970          LD   L,A
0B18 78           3980          LD   A,B
0B19 9C           3990          SBC  H        REGISTER A CONTAINS X
0B1A 67           4000          LD   H,A      H=XY/8
0B1B 29           4010          ADD  HL,HL
0B1C 29           4020          ADD  HL,HL
0B1D 29           4030          ADD  HL,HL
0B1E 7C           4040          LD   A,H
0B1F 29           4050          ADD  HL,HL
0B20 CA 3B 0B     4060          JP   Z,ID1
0B23 F2 3D 0B     4070          JP   P,ID2
0B26 84           4080          ADD  H
0B27 2F           4090          CPL           COMPUTE FF DELAY
0B28 C6 01        4100          ADD  1        ADD 1 FOR 2'S COMP
0B2A FA 32 0B     4110          JP   M,ID3
0B2D FE 03        4120          CP   3        GREATER THAN THRESHOLD?
0B2F FA BC 0A     4130          JP   M,RD5    NO
0B32 CD 7A 0A     4140 ID3      CALL FF
0B35 C3 BC 0A     4150          JP   RD5
0B38 1C           4160 ID1      INC  E        Y=0?
0B39 1D           4170          DEC  E
0B3A CA 45 0B     4180          JP   Z,RD6    YES
0B3D 84           4190 ID2      ADD  H
0B3E 07           4200          RLCA
0B3F C6 05        4210          ADD  5
0B41 C3 CC 0A     4220          JP   FRCOR
0B44 00           4230          NOP
0B45 42           4240 RD6      LD   B,D       COUNT
0B46 D1           4250          POP  DE        RETRIES, MODE
0B47 C5           4260          PUSH BC        COUNT
0B48 2A B3 0A     4270          LD   HL,(POINTR)
0B4B E5           4280          PUSH HL
0B4C 21 00 00     4290          LD   HL,0D  RESET CRC
0B4F CD 15 0A     4300 RD56     CALL GET
```

```
0B52 1C          4310        INC  E
0B53 1D          4320        DEC  E
0B54 C2 5F 0B    4330        JP   NZ,RD55
0B57 E3          4340        EX   (SP),HL SWITCH CRC,POINTER
0B58 71          4350        LD   (HL),C STORE DATA
0B59 23          4360        INC  HL      BUMP POINTER
0B5A E3          4370        EX   (SP),HL SWITCH CRC, POINTER
0B5B 05          4380 RD55   DEC  B       DECREMENT COUNT
0B5C C2 4F 0B    4390        JP   NZ,RD56
0B5F C1          4400        POP  BC      ADJUST STACK POINTER
0B60 C1          4410        POP  BC      COUNT
0B61 CD 15 0A    4420        CALL GET
0B64 CD 15 0A    4430        CALL GET
0B67 DB 02       4440        IN   TAPEIN STATUS
0B69 1F          4450        RRA          OVERRUN?
0B6A DA 7B 0B    4460        JP   C,ALTRD YES
0B6D 1F          4470        RRA  A
0B6E 1F          4480        RRA  A       STOP?
0B6F DA 96 0B    4490        JP   C,RD11 YES
0B72 97          4500        SUB  A
0B73 84          4510        ADD  H
0B74 C2 7B 0B    4520        JP   NZ,ALTRD NO
0B77 85          4530        ADD  L
0B78 CA 85 0B    4540        JP   Z,RD19
0B7B 3E 05       4550 ALTRD  LD   A,5D   GREATER THAN 1 BLOCK
0B7D CD 68 0A    4560        CALL FR
0B80 3E 01       4570        LD   A,1D   ERROR=1
0B82 C3 F1 0A    4580        JP   RD8
0B85 50          4590 RD19   LD   D,B    SAVE COUNT
0B86 15          4600        DEC  D      DECREMENT SAVED COUNT
0B87 CD 15 0A    4610 RD9    CALL GET
0B8A 14          4620        INC  D      INCREMENT SAVED COUNT
0B8B C2 87 0B    4630        JP   NZ,RD9
0B8E 97          4640        SUB  A      ERROR=0
0B8F C9          4650        RET
0B90 E6 04       4660 RD10   AND  04H    STOP?
0B92 CA F6 0A    4670        JP   Z,RD52 NO
0B95 D1          4680        POP  DE     RETRIES, MODE
0B96 CD 4F 0A    4690 RD11   CALL REWIND
0B99 3E 03       4700        LD   A,3D   ERROR=3
0B9B C3 F1 0A    4710        JP   RD8
```

H. PHIDECK MAINTENANCE

Recommended Field Maintenance

This maintenance schedule consists of recommended maintenance operations to be performed in the field by operating personnel and service technicians. Schedule A consists of cleaning operations that should be performed every ten to twenty hours of operating time. Since the accumulation of dirt and tape oxide is highly dependent upon operating environment and the quality of tape used, the time interval for Schedule A can be varied according to system experience. The Schedule A cleaning operations are simple enough that they can be performed by operating personnel in many systems.

The items in Schedule B should be performed by technically skilled personnel.

Required Equipment For Schedule A

1. Tape head cleaner or pure isopropyl alcohol
2. Rubber drive cleaner
3. Cotton tip wood swabs (Q-Tips)
4. Soft bristled brush
5. Tape head demagnetizer

Schedule A (10 to 20 hour intervals)

1. Remove accumulated dust, tape oxide particles, etc. with a soft bristled brush.
2. Clean magnetic head and tape guides with tape head cleaner or isopropyl alcohol.
3. Clean the capstan shaft with a cotton tip swap moistened with tape head cleaner. **Do not allow** tape head cleaner to run down the capstan shaft into the capstan bearing. Use only enough cleaning liquid on the cotton tip swab to remove tape oxide from the exposed portion of the capstan shaft.
4. Clean pinch roller with rubber drive cleaner or isopropyl alcohol.
5. Demagnetize the tape head using a tape head demagnetizer.

Schedule B (500 hour intervals)
Maintenance Guide

This maintenance schedule consists of recommended maintenance checks and operations to be performed in a facility equipped for tape deck repairs and maintenance. For greatest system reliability, this procedure should be performed on a regular basis at intervals of approximately 500 hours of tape deck operating time. Where such maintenance is not performed on a scheduled basis, this routine should be performed whenever a tape deck is returned to a repair facility for repairs.

Required Equipment

1. Tape head cleaner or pure isopropyl alcohol
2. Rubber drive cleaner
3. Lightweight machine oil
4. SAE 10 wt. oil
5. Cotton tip wood swabs (Q-Tips)
6. Soft bristled brush
7. Tape head demagnetizer
8. Information Terminals M-300 Tape head and guide gauge set
9. Oscilliscope
10. Speed test tape
11. Miscellaneous hand tools
12. Frequency counter

Cleaning

1. Clean Phideck throughly. Remove accumulated dust, tape oxide particles and lint with air hose or brush.
2. Demagnetize tape head
3. Clean tape head and tape guides with liquid cleaner and cotton swab. Use only a commerical tape head cleaning fluid or pure isopropyl alcohol.
4. Clean capstan shaft with a cotton tip wood swab moistened with tape head cleaner. Do not allow tape head cleaner to run down the capstan shaft into the capstan bearing. Use only enough cleaning liquid on the cotton swab to remove tape oxide from the exposed portion of the capstan shaft.
5. Clean capstan drive rubber roller. Use rubber drive roller cleaner or pure isopropyl alcohol.

Lubrication

1. Oil the headbar pivot bushings using a drop or two of SAE 10 weight oil. Wipe off excess oil.
2. Apply a drop of lightweight machine oil to the capstan bearing where the capstan shaft enters the bearing. Clean any excess oil from the capstan shaft.

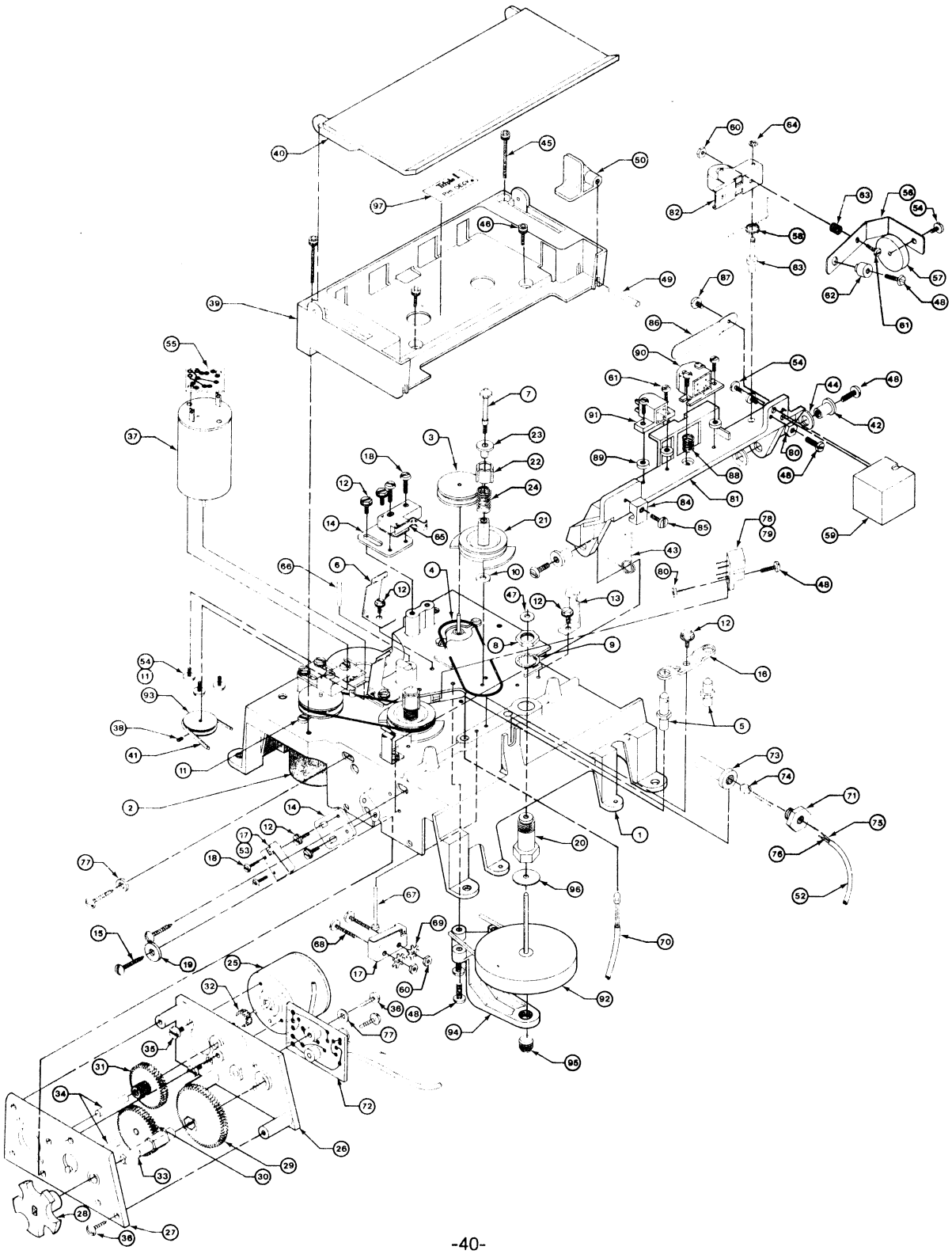
Drive Belts

1. Remove the plastic cassette well and check the two reel drive belts. The belts should be replaced if there are any signs of splitting, cracking, or wear.
2. Check the belts for slippage by stalling the associated reel post while in the Fast Forward mode for the takeup reel and Rewind mode for the rewind reel. The belts should be replaced and the pulleys cleaned if there is belt slippage during the stalled condition.
3. Check the capstan flywheel drive belt for cracking, splitting, or wear. Replace if necessary.

Alignment Checks and Adjustments

1. Using the Information Terminals M-300 gauge set and with the headbar engaged, check head depth of penetration, zenith and guide height. The parameters being out of tolerance indicate that the gearbox positioning may need to be adjusted to compensate for starwheel assembly wear.
2. If the previous checks indicate head misalignment due to gearbox positioning, perform gearbox assembly alignment procedure. If head alignment is correct, do not perform adjustment.
3. Check gearbox starwheel to headbar engage-disengage positioning. Adjust starwheel position sensing micro-switch for correct positioning if necessary.
4. Check pinch roller pressure and adjust if necessary.
5. Using a high quality tape with a continuously recorded tone or flux reversal pattern, check the play or read head output for signal levels and quality. Incorrect signals are indicative of head wear, head alignment or tape tracking problems.
6. Check tape speed and adjust as described in the Motor Speed Calibration paragraph in section VI.
7. Check and adjust the head azimuth as described in the Head Azimuth Adjustment paragraph in section VI.

PHI-DECK® EXPLODED VIEW

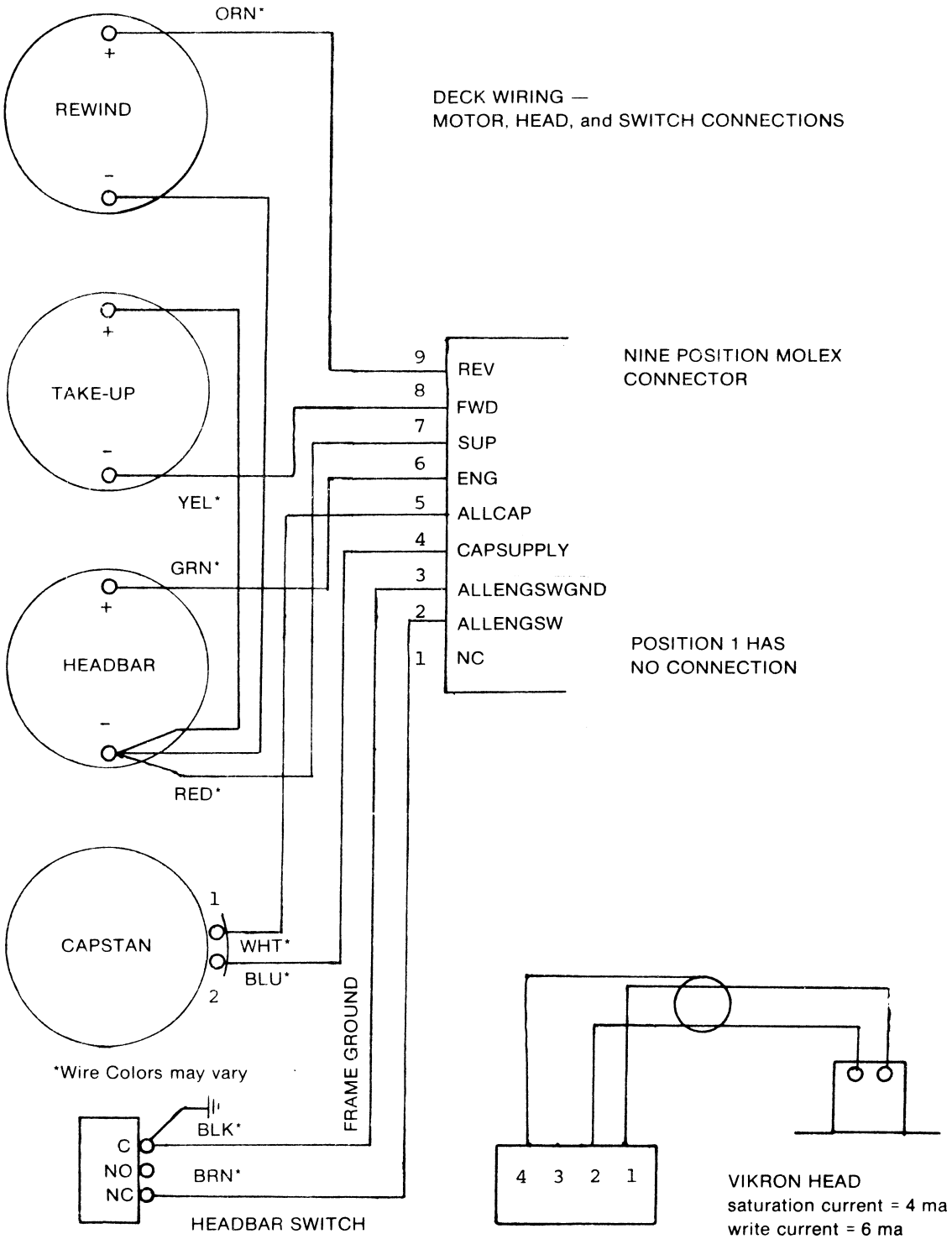


PHIDECK PARTS MATRIX

Item No.	Description	Quantity
1	Cast Chassis	1
2	Reel Motor	2
3	Reel Motor Pulley	2
4	Reel Motor Belt	2
5	Cassette Guide Post	2
6	Rear Spring	2
7	Reel Rest Post	2
8	Bearing Housing Nut	1
9	Lock Washer	1
10	Spacer	2
11	Machine Screw, Metric	8
12	Machine Screw	5
13	Side Spring	2
14	Plate	1
15	Sheet Metal Screw	3
16	Guide Post Clamp	1
17	Snap-action Switch	1
18	Machine Screw	2
19	Flat Washer	1
20	Bearing Assembly	1
21	Optic Reel Rest	2
22	Reel Rest Slider	2
23	Reel Rest Sleeve	2
24	Reel Rest Spring	2
25	Gearbox Motor	1
26	Gearbox Side Assembly "A"	1
27	Gearbox Side Assembly "B"	1
28	Starwheel	1
29	Gear	1
30	Gear	1
31	Gear	1
32	Pitch Pinion Gear	1
33	Starwheel Shaft	1
34	Gear Shaft	2
35	Machine Screw, Metric	2
36	Sheet Metal Screw	1
37	Capstan Drive Motor *	1
38	Set Screw	1
39	Cassette Well	1
40	Cassette Well Door	1
41	Capstan Drive Belt	1
42	Headbar Pivot Sleeve	2
43	Headbar Pivot Spring	1
44	Headbar Pivot Spacer	2
45	Allen Head Screw	2
46	Allen Head Screw	2
47	Dust Protector	1
48	Machine Screw	6
49	Eject Lever Pin	1
50	Eject Lever	1
51	Wire Harness Assembly *	1
53	Heat Shrink Tubing (inches) *	1.5
61	Machine Screw	4
64	E-Ring	1
77	Flat Washer	1
80	Nut	1
81	Headbar	1
82	Pressure Roller Assembly	1
83	Pressure Roller Post	1
84	Cable Clamp	1
85	Machine Screw	1
86	Pressure Roller Spring	1
87	Machine Screw	1
88	Head Azimuth Spring	1
89	Head Spacer	X
90	Read/Write Head	X
92	Flywheel Assembly	1
93	Capstan Pulley 5IPS	1
94	Flywheel Bracket	1
95	Nylon Set Screw	1
96	Flywheel Washer	1
97	Triple I Label	1

* Item not shown

I. Phideck Wiring



NOTE: Four position Molex connector may be cut between 2 and 4 to separate HDGND from HDB and HDA.

1. HDB
2. HDA
3. No Connection
4. HDGRND (Shield)

J. PHIDECK CONNECTIONS STANDARDS

In an effort to maintain compatibility between Digital Group systems using Phidecks, complete wiring diagrams have been included for connecting Phidecks to your system. Refer first to the Phideck system block diagram to locate the appropriate wiring diagram. A brief explanation of each diagram is included.

DETAIL 1: This diagram details the motherboard connections between the I/O Port card and the Phideck card using the wire wrap pins on the 36 pin connector of each board.

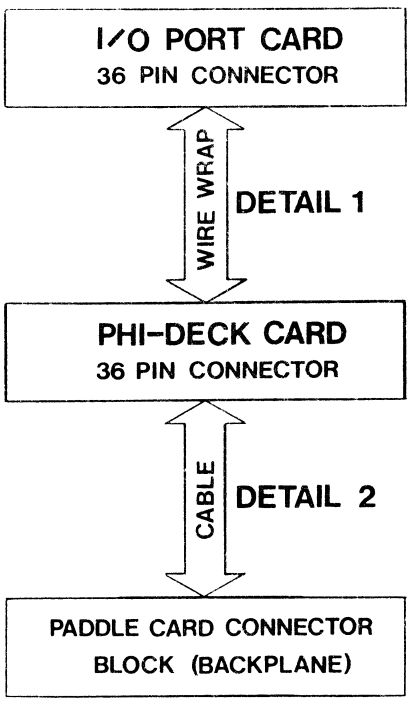
DETAIL 2: The connections between the backplane of the paddle card connector block and the Phideck card 36 pin connector are detailed on this diagram. Complete the wiring as if your system were using four Phidecks, even if you are using less than four decks. There are several wires in the cable for decks 1 and 3 that are common to all the decks. The best approach is to make-up cables with molex connectors on each end that slip over the wire wrap pins. If you should prefer not to use this method, please refer to Appendix C for the actual Phideck card pinout.

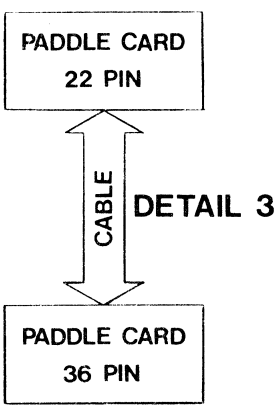
DETAIL 3: This detail shows the cabling between the paddle card going to the CPU cabinet (22 pin) and the paddle card going to the Phideck cabinet (36 pin). There are two groups of wires on this diagram. Shielded cables should be used for the group on the left, since this cable contains the tape head signals. Also note that the shield from the shielded cable doesn't go to chassis ground, but is strictly ground for the tape heads to help avoid noise on the head ground. Ribbon cable (20 conductor) works best for the group on the right.

DETAIL 4: Phideck cabinet wiring is detailed in this diagram. Your wiring needs will depend on the number of Phidecks in your system. The Phidecks are numbered Ø thru 3, so if you are using only one Phideck, connect the cables labeled for deck Ø.

The Digital Group strongly recommends you follow the interconnect standards. This will greatly facilitate repair of your system, should you find it necessary to return it for service. If you send us your system please detail the connections on the paddle card connector block, etc. or state that you are following the Digital Group standard.

PHI-DECK SYSTEM BLOCK DIAGRAM

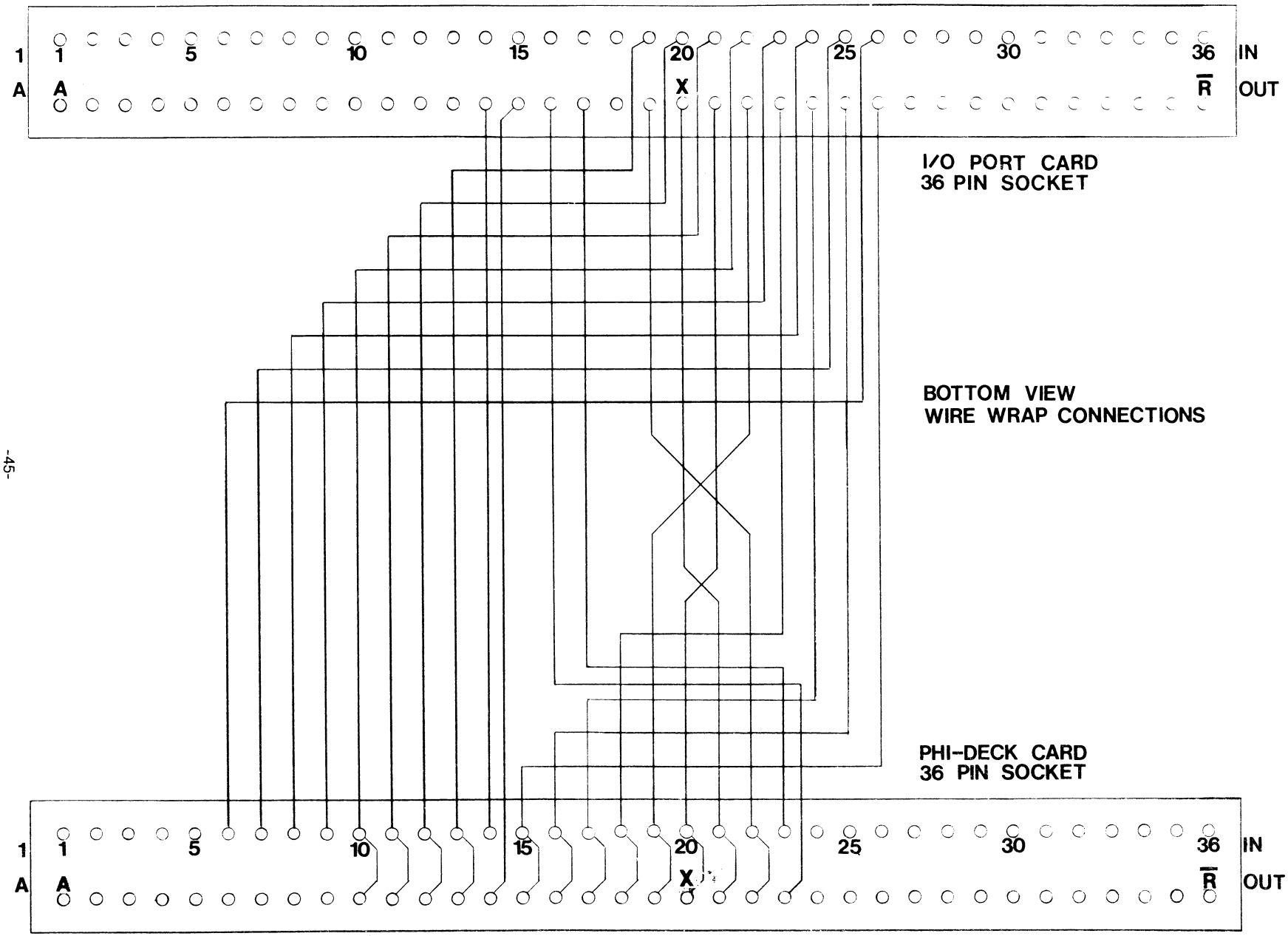




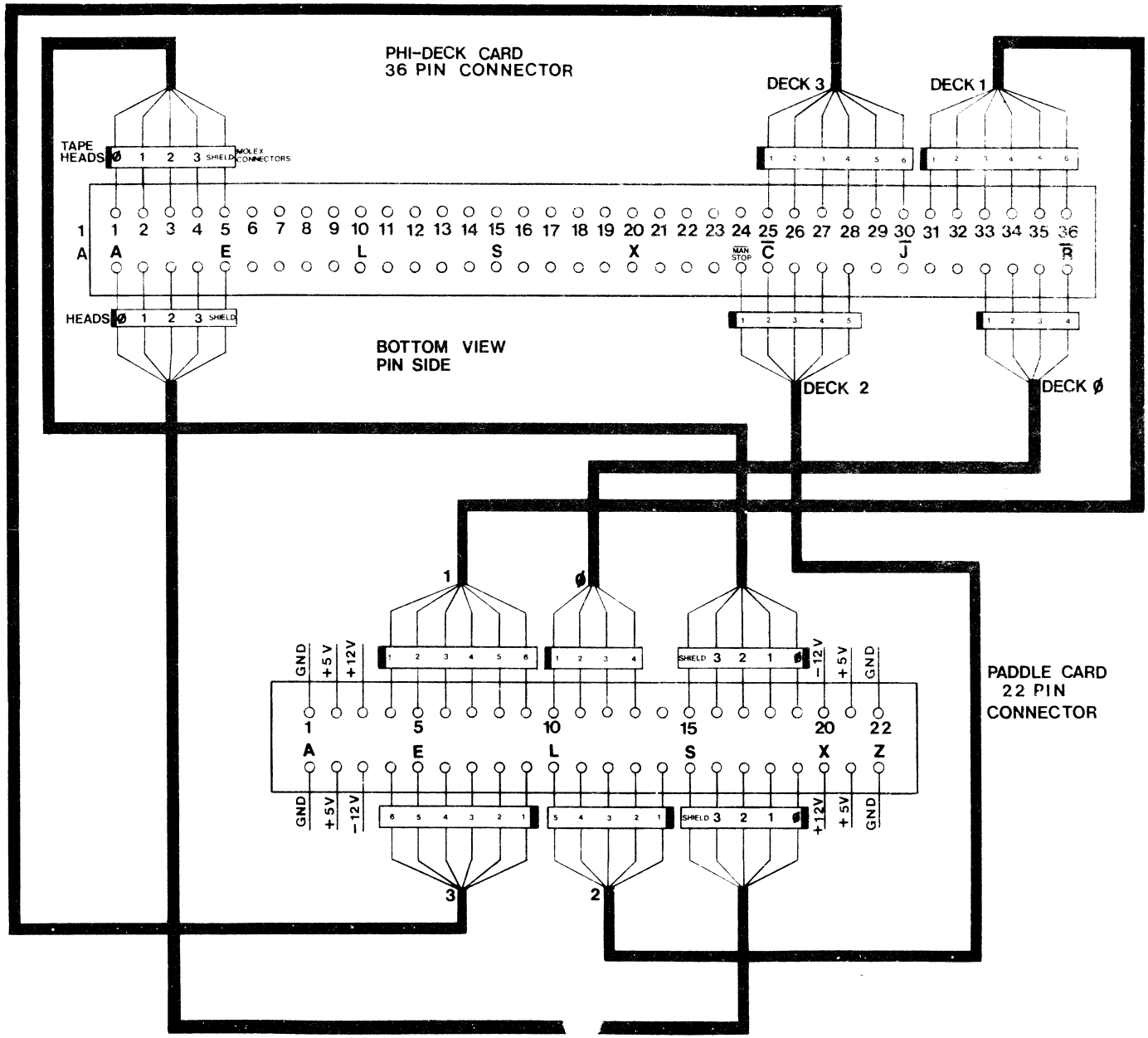
PHI-DECK CABINET WIRING

DETAIL 4

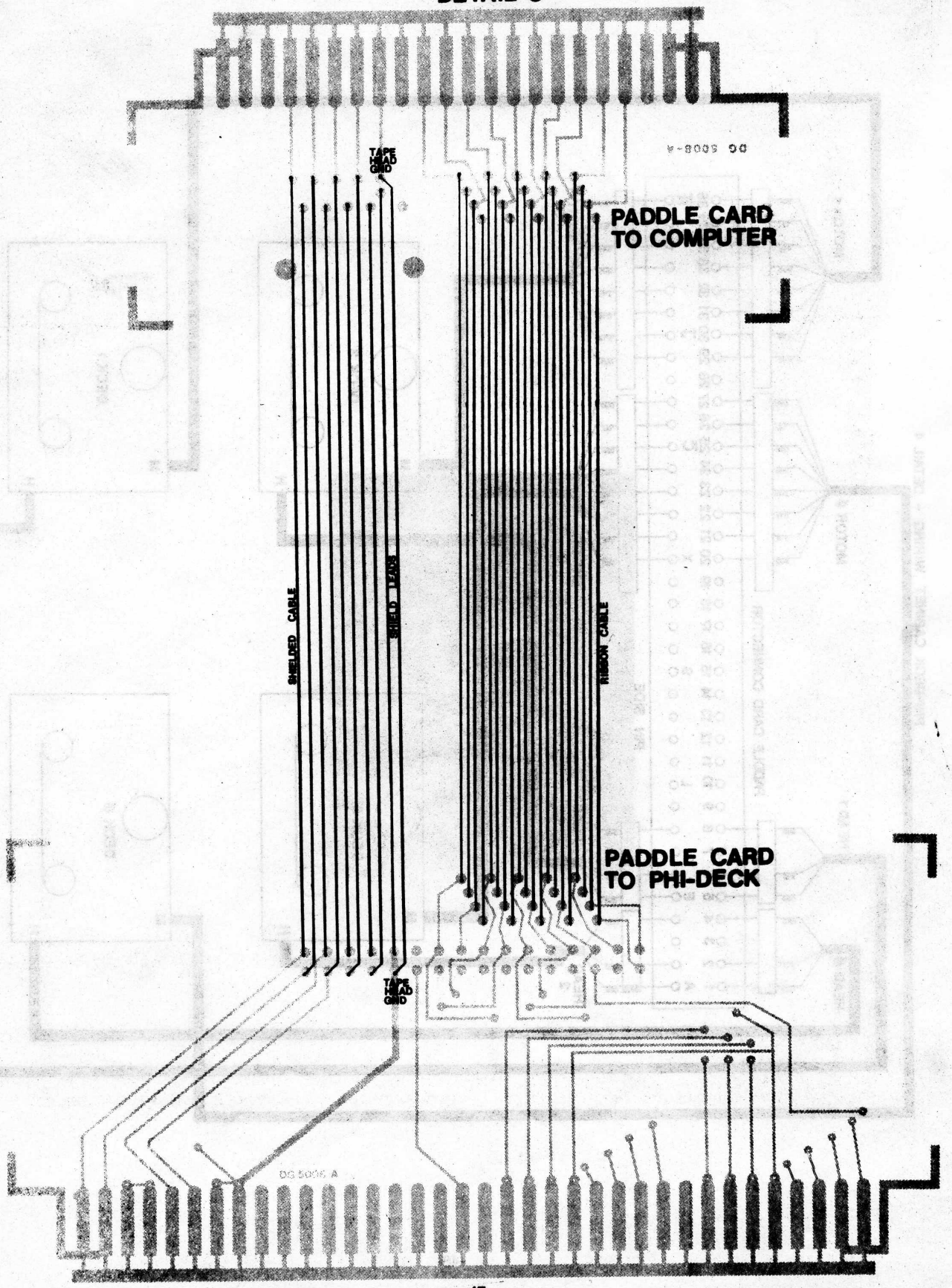
CONNECTIONS BETWEEN CARDS - DETAIL 1

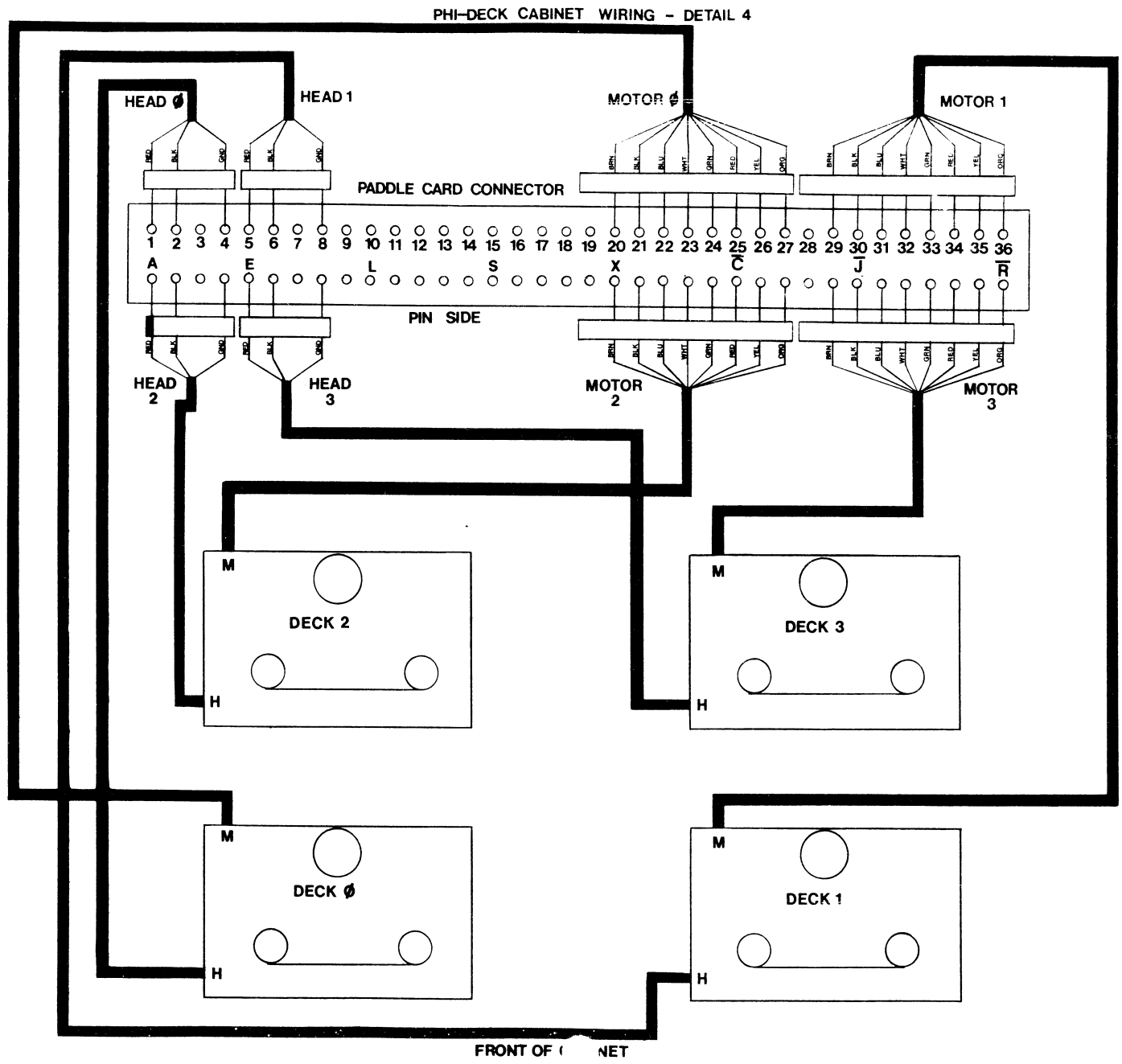


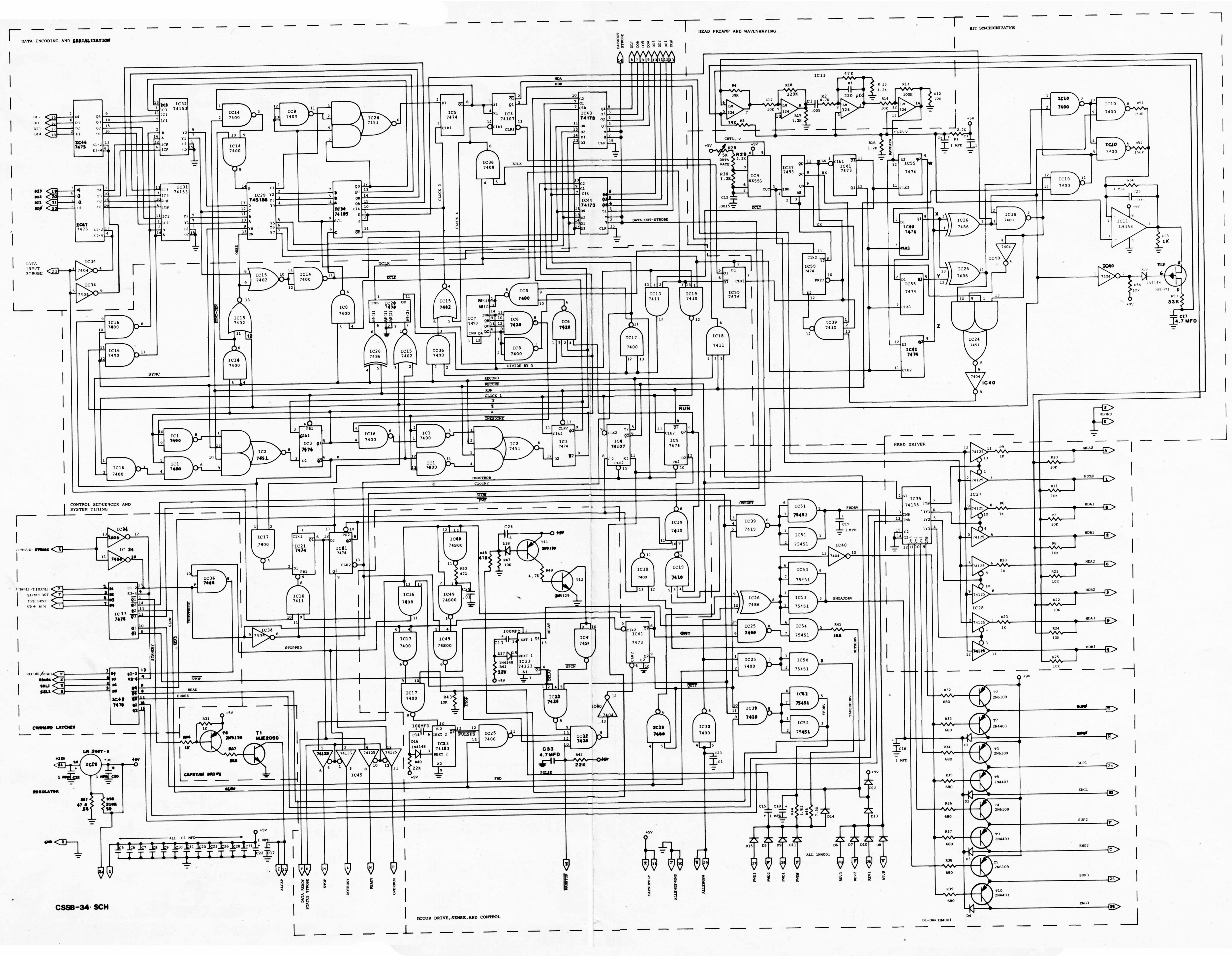
PHI-DECK CARD CONNECTIONS TO
PADDLE CARD BACKPLANE - DETAIL 2



DETAIL 3


TAPE HEAD GND
PADDLE CARD TO COMPUTER
SHIELDED CABLE
RIBBON CABLE
PADDLE CARD TO PHI-DECK
TAPE HEAD GND


PHI-DECK CABINET WIRING - DETAIL 4
HEAD Ø
HEAD 1
MOTOR Ø
MOTOR 1
PADDLE CARD CONNECTOR
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36
A E L S X C̄ J R̄
PIN SIDE
HEAD 2
HEAD 3
MOTOR 2
MOTOR 3
M
H
DECK 2
DECK 3
DECK Ø
DECK 1
FRONT OF


DATA ENCODING AND SERIALIZATION
HEAD PREAMP AND WAVESHAPING
BIT SYNCHRONIZATION
HEAD DRIVER
CONTROL SEQUENCER AND SYSTEM TIMING
COMMAND LATCHES
CAPSTAN DRIVE
REGULATOR
MOTOR DRIVE,SENSE,AND CONTROL
DATA-OUT-STROBE
DATA INPUT STROBE
D1-D4= 1N4001
ALL 1N4001
CSSB-34 SCH

PHI-DECK CONTROLLER INTERFACE