the digital group
po box 6528 denver, colorado 80206 (303) 777-7133

THE 32K DYNAMIC MEMORY BOARD

298-119

Digital Group 32K Dynamic Memory Card

Introduction

The Digital Group 32K x 8 Dynamic Memory card uses the 4K x 1 16-pin dynamic memory chip of the 4027 or equivalent type. Sixty-four of the ICs are required. The card is designed to plug into a Digital Group Z-80 system. Two of these cards will make up the whole 64K that the Z-80 can use.

The 4027 or equivalent is a 16-pin dynamic memory. The small size of these ICs permits placing 64 on a single 5" x 12" card, along with the decoders and drivers. Three voltages are required (+5V, +12V, -5V); +5V @ 6A supply in a Digital Group system would run a 64K system. The 4027 uses 6 address lines which are multiplexed to provide 12 lines ($2^{12} = 4096$) for 4K of address space. The 6 address line sets are designed so that a $\overline{RAS}$ strobe sets in the lower 6 addresses, and a $\overline{CAS}$ strobe sets in the next 6 addresses. In the case of a Read operation, the data will be available approximately 200 ns later. A Write operation requires a Write strobe in addition.

Dynamic memories have a major disadvantage: they require a set of 64 refresh signals at least every 2 milliseconds. Fortunately the Z-80 will automatically supply these refresh signals.

The 32K dynamic card provides on-card jumpering for allocating the card as lower or upper memory (0-32K or 32K-64K). Another jumper selects each refresh command or every fifth refresh command from the Z-80 card. Using every fifth refresh will still provide adequate refreshing, but will considerably reduce power supply requirements.

Full input, output, address and command buffering is featured on this card.

The 32K dynamic memory card may be used along with either 8K static memory cards or a 32K static memory card. The 32K dynamic memory card will take priority in any memory overlap condition except for EROM and ROM.

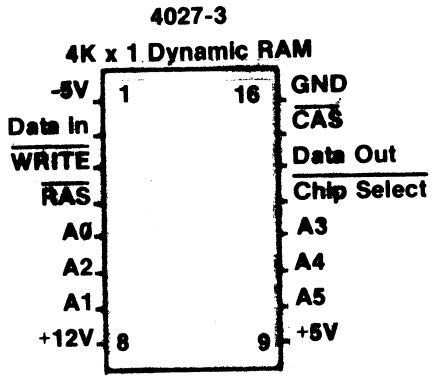


FIGURE 1 — RAM Chip Pinout

(Top View)

Circuit Description

The memory configuration of the 32K dynamic memory card is similar to that used in the Digital Group 8K x 8 static memory cards. To obtain 8-bit bytes or data words used by the CPU, memory chips are grouped by rows (or banks) of eight. By tying the $\overline{RAS}$ lines of each chip in a bank together, the memory ICs of a bank are simultaneously enabled. All chips have their $\overline{Chip\ Select}$ pin grounded. This results in a $\overline{RAS\ Chip\ Select}$ system which uses less power supply current. Each chip of a particular bank provides one bit of an 8-bit word, i.e., IC00 provides Bit 0 (LSB), IC01 provides Bit 1, and so on, with IC07 providing Bit 7 (MSB).

Refer to the schematic and parts layout diagram for IC numbering and placement.

IC00-IC77 are the memory chips. The first digit refers to the bank of memory, and the second digit is the chip's bit location. For example, IC47 is the bit 7 (MSB) RAM in bank 4.

IC86 and IC88 (74125s) are data bus drivers for the eight lines to memory. IC85 and IC89 (74125s) are bus drivers for the eight data output lines from memory going to the CPU. The output drivers are enabled whenever a memory request is made of the memory area assigned to this card. This will occur when the output pin 12 section of the 7410 (IC84) goes low.

The four most significant address lines are brought into a 7475 (IC90) data latch. The $\overline{Memory\ Request}$ line going low, slightly delayed, strobes these four address lines into the 7475. This address holding latch is required due to a potential data glitch occurring in the Z-80 chip. The latched output of the 7475 goes to a 7442 (IC91) decoder which selects the 8 banks to be accessed. A pair of 74S08s (IC87 and IC92) provide the $\overline{RAS}$ (Row Address Strobe) to the appropriate bank of memory. The $\overline{RAS}$ is used both for accessing and refreshing the memory.

When Z-80 refreshing is desired, the $\overline{Refresh}$ line will go low. The $\overline{Refresh}$ line clocks the input to the 74193 (IC82). The output pin 12 section of IC83 (74L04) provides a reset pulse to the 74193 counter either after each $\overline{Refresh}$ signal or every fifth $\overline{Refresh}$ signal. Reduced memory current requirements occur when only every 5th Refresh is used, but a marginal memory could fail under these conditions. The $\overline{Refresh}$ signal is gated by the $\overline{Memory\ Request}$ line and applied to all of the $\overline{RAS}$ lines of the memories. The address being refreshed will appear on the six least significant address lines. The refreshing action is completely automatic and begins as soon as power is applied. $\overline{Refresh}$ does not occur during $\overline{Reset}$ time, $\overline{Wait}$ time, or the $\overline{Bus\ Request}$ time of the Z-80 CPU.

The general accessing of memory operations to Read or Write memory consists of rather critically timed strobe signals. Three (four in the case of Write) strobes are required. This strobing action is generated by the $\overline{Memory\ Request}$ signal coming from the Z-80 CPU. The first operation to occur is $\overline{RAS}$ to the selected bank. During $\overline{RAS}$, the two 74L157 (IC79 and IC80) multiplexers select the 6 least significant address lines. An 8T97 (IC78) drives the address lines of the memories. The $\overline{RAS}$ signal on pin 4 of the driven bank of 4027s will last about as long as the $\overline{Memory\ Request}$ signal, although slightly delayed by about 20 ns. After 60 ns, pin 1 of the 74L157s will go low, and the next upper 6 bits of memory (LSB+6 to LSB+11) will be selected. 80 ns later the $\overline{CAS}$ (Column Access Strobe) occurs. The full 12 bits of address (2^{12} = 4096 [4K]) have now been entered into the system. Depending on the accessing speed of the memories used, the data at the addressed cell will soon become valid and available at the output pin 14 of the memories.

Dynamic memories are more susceptible to noise than static memories. For this reason, a large quantity of bypass condensers are used to surpress transients at $\overline{RAS}$ and $\overline{CAS}$ time. In addition the three power supplies and ground lines to the memories are gridded to produce the lowest impedence at the power pins of the memories. The 74L157s reduce any noise on the address lines, as well as introducing required delays. The condenser (C2) and the 74L04 also produce strobe delays.

The power requirements vary greatly according to chip access and manufacturer, as well as the number of refreshes and accesses performed.

Assembly

Estimated Construction Time: 2-6 hours.

To build The Digital Group 32K Dynamic Memory Card, you will need the following tools and equipment:

Fine tipped low wattage soldering iron (approximately 25 watt)
Solder—60/40 resin wire solder, 20-30 gauge
Do not use acid core solder!
Diagonal cutters—small micro-shear type preferred
Long-nosed pliers
Flux remover or alcohol
Small brush
Volt-ohm meter

Refer to the parts placement diagram during construction.

Before you begin to mount and solder components, inspect the memory card. **The side from which the components are mounted has the Digital Group label on the bottom left portion of the card.** Compare the areas where IC sockets will be inserted with the layout to see that there are no shorts occurring between either the traces leaving the IC or the IC pads or holes in which the ICs are mounted. Once the IC sockets are inserted it is very difficult to find such a problem.

The sockets should be mounted as close to the card as possible. Do not bend the leads of the IC sockets excessively before soldering, as they may break off at the base of the socket.

☐ Check all components provided with the parts list and the parts placement diagram.

☐ Install and solder the 16-pin IC sockets on the card. On 16K cards, only the memory ICs on the left side are installed.

3	Resistor-pack sockets	RP1, RP2, RP3
6	Memory support IC sockets	IC78-80,82,90,91
64 (32 on 16K card)	Memory IC sockets	IC00-77 (IC00-37 on 16K version)

☐ Install and solder the 14-pin IC sockets on the card.

9	Memory support IC sockets	IC81,83-89,92

☐ Install and solder the 2.2K resistor pack (10-pin SIP) on the card. Note the dot on one end. This end must be oriented towards the top nearest IC83.

1	2.2K resistor pack (SIP)	SIP 1

☐ Install and solder capacitors on the card and clip excess leads. On 16K cards four .01mfd capacitors, C86, C89, C92, and C95, on the right side of the card are not installed. Also the 40 .1 mfd capacitors shown on the memory array on the right side are not required on 16K cards.

13(9)	.01 mfd ceramic disc capacitors	C83-C95
80(40)	.1 mfd ceramic disc capacitors	C3-42, 43-82
1	100 pfd, mica capacitors	C1
1	330 pfd, mica capacitor	C2
3	22mfd, tantalum (note polarity)	C96,97,98

☐ Install and solder jumpers on the card, using thin wire or leads obtained from previous steps.

1	Refresh or Refresh/5 ($\overline{R}$ or $\overline{R/5}$) jumper	($\overline{R}$ recommended)
1	Memory designation, upper or lower	(Upper memory designation recommended)

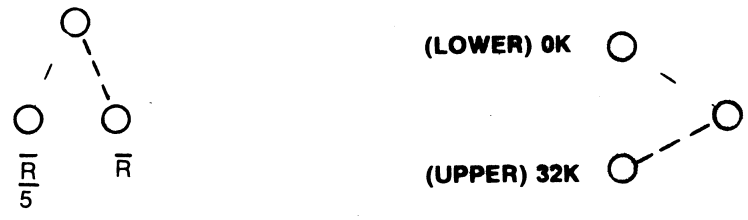


FIGURE 2 — Memory Card Jumpers

- ☐ Measure the resistance between pin 1 (+5V DC) and pin 2 (GND) on the card edge connector with an ohmmeter. Numbering on the card is from 1 to 36 on the component side of the card starting from the left. On the circuit side of the card labeling is from A to R, pin 1 opposite pin A and pin 36 opposite R. Similarly measure between pin 36 (+12V DC) and pin 2, and between pin b (-5V DC) and pin 2.

  A low resistance reading indicates a bad capacitor or a solder bridge "short" somewhere on the card.

- ☐ Insert ICs 78 through 92 (and the three 16-pin R-packs) in the center of the card. Again measure the resistance between connector pins 1 and 2. Reverse the meter leads and compare readings with the reverse polarity. The resistance should be somewhat lower in one direction than the other, but not zero ohms. The same resistance in each direction indicates a reversed IC.

Memory Insertion and Diagnosis

The memory ICs are essentially connected in parallel by the address and data lines, and therefore can represent a considerable "guessing game" if all of the memory chips were to be inserted along with one defective or shorted chip. However, don't try installing just a few chips as the capacity effect of the ICs affects $\overline{RAS}$ and $\overline{CAS}$ timings. A preferred technique is to insert one half at a time and test with an optional cassette, the 32K dynamic memory test tape for Z-80 systems. **Note:** The 16K Digital Group memory tests developed for static memory may erroneously indicate errors.

1. Start by inserting IC00 through IC37 in the sockets at the top left of the card as shown on the layout, with the notch or pin 1 end away from the connector. (The bank and IC numbering scheme of the Digital Group 32K memory card is not the same as the Digital Group 8K memory card!) Insert the card into your CPU cabinet and run the dynamic memory test program.

2. After successfully testing the first half of memory with the memory test routine, continue by inserting the rest of the memory ICs and test in the same manner. You must always completely populate a bank to test with the memory test tape.

3. Once the card is populated, it is advisable to run an extensive memory test (2-3 days continuously) with the dynamic memory test tape. Chip failure (fallout) occurs most frequently in the initial hours of operation. Chips which are temperature sensitive also will fail or be indicated by an extensive memory test.

4. The ICs used on the memory card can also be rather sensitive to the power supply voltage. To insure that your system remains error-free, adjust the +5 volt supply to measure between 4.5 and 5 volts at the memory supply bus on the 32K memory cards (between pin 1 and pin 2). Note that additional cooling often solves other strange memory problems.

Using the 8K Memory Test Supplied with the Z-80 Operating System

When the Dynamic Memory Test #2 finds a missing or bad IC, or unsoldered or bent pin, the card number (0 or 1) and the IC number (00 - 77) will be printed on the screen, as "B1 IC15". BØ refers to a 0-32K card designation and B1 refers to a 32K - 64K card designation.

The memory test included with the 64 character TV Z-80 operating system can be used although it may sometimes give erroneous results, particularly upon entering a new memory bank. The 32K dynamic memory test program corrects the problem which occurs in the Z80 OP System memory test. The 32K dynamic memory test program can be used on static memory cards. 8K cards will require some translation to find the bad IC number.

Troubleshooting

The 32K dynamic card is best analyzed by assigning an individual 32K dynamic card to the memory space of 32K-64K (jumpers as shown in Figure 2). Additionally, at least 8K of tested memory (static or dynamic) should be assigned 0-8K. The 32K dynamic memory test program is then loaded and run. The TV screen will display a + sign as long as memory tests okay. In case of any error, the failing address and the offending IC# or decoder/driver will be indicated on the screen. Run the memory tester periodically, especially before any major software operation.

Several procedures are recommended in case of error. In the case of a new or repaired card, the failure is frequently caused by soldering or manufacturing defects. Most frequently the trouble will be an unsoldered pin, or a pin bent underneath the IC when it was inserted into the socket. A problem occurring in an older card is generally caused by an IC gone bad. Of course, there are just enough exceptions to keep things exciting.

A decoder/driver caused problem is generally the most difficult. An oscilloscope is almost mandatory at this point. Additionally, short software programs which exercise the decoder will permit viewing the timings drawn in this document. The program used to obtain the patterns shown in Figure 3 is listed below:

Address	Data	Operation	
005250	041	Ld HL,200000	Set to beginning of dynamic memory
005251	000		
005252	200		
005253	176	Ld A,(HL)	Read the memory
005254	043	Inc HL	Reset memory address
005255	174	Ld A,H	Check memory page address
005256	376	CP 220	Check only 32K-36K
005257	220		(Bank IC00-IC07)
005260	302	NZ 005253	Continue until @ 36K
005261	253		
005262	005		
005263	303	JP 005250	Start again at 32K
005264	250		
005265	005		
005100	250		
005101	005		

Press option Ø and then look for the patterns as shown. The patterns will be the most stable when triggered by $\overline{CAS}$ going low, with a delayed sweep oscilloscope.

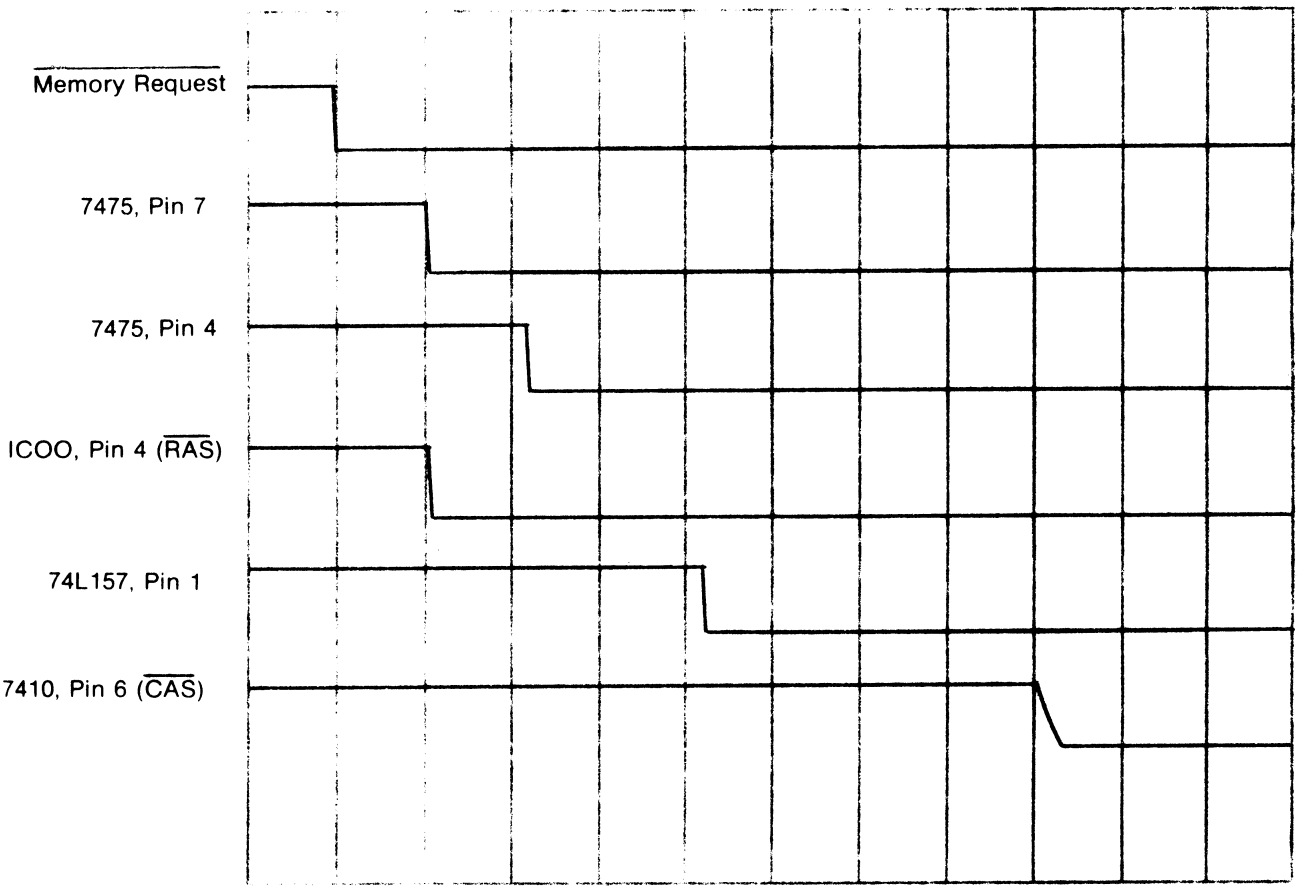


FIGURE 3 Dynamic Memory Access Timing Patterns (20 nsec/div)

CPU Modifications for Use with the 32K Dynamic Boards

As mentioned previously, three cases arise which may cause loss of memory. In each case, the loss of the automatic Refresh system of the Z-80 is the trouble. The Z-80 should never stop Refresh commands for more than one millisecond.

The biggest troublemaker is the $\overline{\text{Reset}}$ line going to the Z-80. When the $\overline{\text{Reset}}$ line is low, the $\overline{\text{Refresh}}$ strobe is turned off. Generally, a fast tap on the Reset button will not cause trouble. No bets, though. A simple modification to the Digital Group Z-80 card will solve the problem. The modification below will give a satisfactorily resetting pulse by utilizing the $\overline{\text{NMI}}$ line. This avoids an internal Z-80 problem that can result in the $\overline{\text{MREQ}}$ line going to an illegal level during a Reset sequence. The $\overline{\text{NMI}}$ Reset system can be quickly implemented by removing R6 (220 ohm) from its original location and placing it between pin 47 and pin AZ. The resistor can be mounted on the component side of the card near the connector and Z-80. Two convenient feed through holes, from pins 47 and AZ next to the connector, can be used.

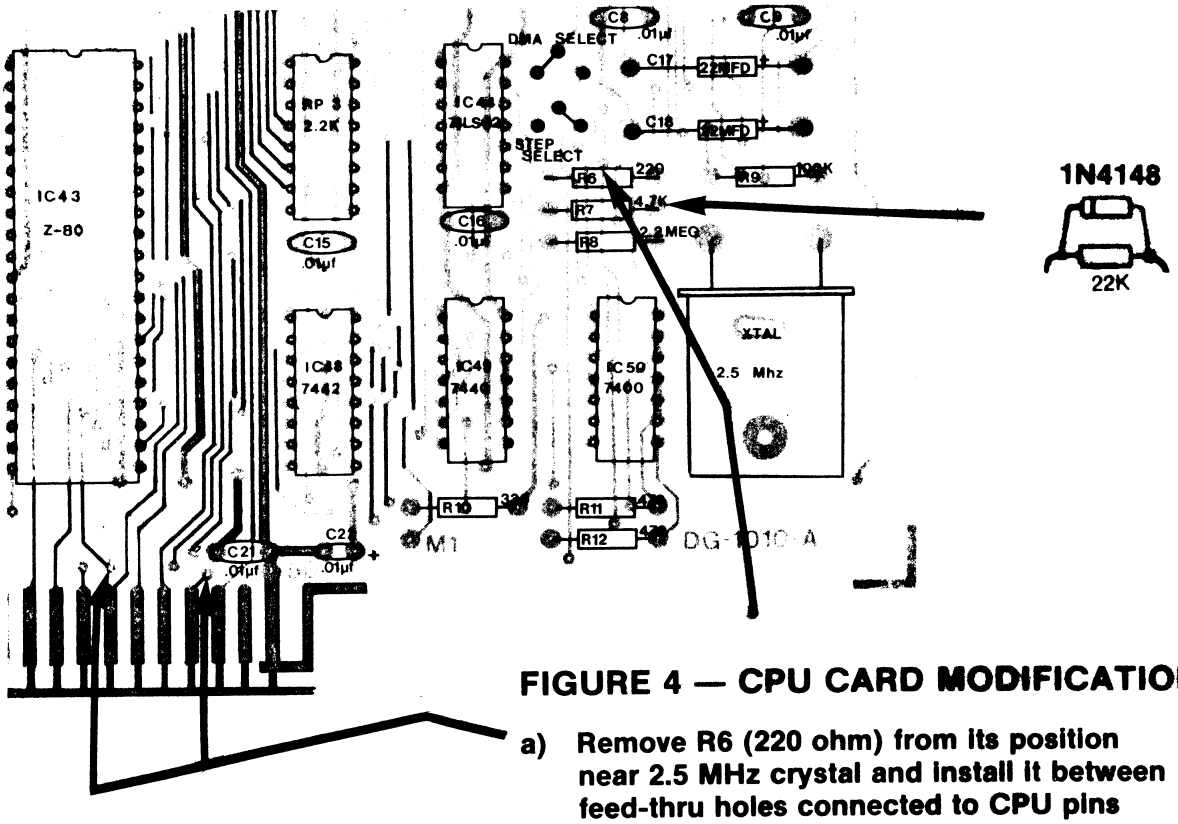


FIGURE 4 — CPU CARD MODIFICATION

a) Remove R6 (220 ohm) from its position near 2.5 MHz crystal and install it between feed-thru holes connected to CPU pins 47 and AZ.

b) Remove R7, 4.7 ohm resistor, and install the resistor-diode combination shown above.

$\overline{\text{NMI}}$ will now occur when the $\overline{\text{Reset}}$ button is pushed. The $\overline{\text{NMI}}$ vector address should then vector eventually to address 000000, the Reset address. The only precaution that should be observed is that an OP System should be loaded before trying to Reset. In practice this means start the cassette recorder, and when the low tone begins, turn on the system. Once powered up and with page 1 loaded, no further concerns about $\overline{\text{Reset}}$ exist.

Front panels will not work with the dynamic memory system, unless designed to also provide the Refresh signal. Similarly other DMA (Direct Memory Access) operations may result in data loss if some system of Refresh is not provided.

Wait state operations are also impacted, e.g., a floppy controller must not tie up the system for more than 1 ms. The system can not be single-stepped through Dynamic RAM areas. The system may be single-stepped through EROM + Static RAM (including stack) areas. Since single-stepping is generally appropriate only for initial CPU diagnosing, non-functioning dynamic memory elsewhere than at the bottom addresses should be no problem.

Dynamic Memories on Floppy-based Systems

The Digital Group floppy disk controller board was originally designed so that whenever data from the floppy was immediately available, the CPU was put into a Wait state. This Wait may be as long as 200 ms, and when the Z-80 is in a Wait state, no Refresh occurs. An RS flip flop can be installed on the floppy disk controller board, along with some simple wiring changes that will result in no excessively long Wait states.

The Reset system on the floppy controller board can cause hang up problems when used along with the required NMI change. A few simple changes eliminate this problem.

Additional Parts Requirements for Floppy/Dynamics Modifications:

2 1N4148 or 1N914
1 7400
3 feet of #30 insulated wire

Detailed Modifications to the Floppy Controller and Digital Group System Motherboard

Refer to Figure 5.

- ☐ Place the floppy controller board pin side up, connectors facing you.
- ☐ Cut the trace going to IC1 pin 8 as shown in Figure 5.
- ☐ Connect a short jumper from IC1 pin 8 to IC1 pin 12 and IC1 pin 13.
- ☐ Connect a short jumper from IC1 pin 11 to the trace originally going to IC1 pin 8.
- ☐ Connect a short jumper from IC1 pin 2 to IC 1 pin 6.
- ☐ Connect a long jumper from IC31 pin 1 to IC1 pin 5.
- ☐ Connect another long jumper from IC21 pin 4 to IC1 pin 1.
- ☐ Connect another long jumper from IC1 pin 3 and IC1 pin 4 to pin C of the dual 36-pin connector.

Refer to Figure 6.

- ☐ Place the floppy controller board component side up, connector facing you.
- ☐ Remove IC1 (7408). Replace with a 7400 IC.
- ☐ Remove R17 (47 ohm).
- ☐ Remove R16 (22K). Save this resistor for later.

Refer to Figure 7.

- ☐ Place the Digital Group motherboard pin side up.
- ☐ Connect a long jumper from pin C of the dual 36-pin connector of the floppy controller card to pin 17 of the dual 36-pin connector of the port Ø to 3 I/O card. The I/O board and the floppy controller board may not be in the pictured locations, but the relative pin locations will be the same.

Refer to Figure 4 (shown previously).

- ☐ Place the Z-80 CPU board component side up, connector facing you.
- ☐ Place a 1N4148 diode around the 22K resistor previously removed.
- ☐ Insert and solder the 22K and 1N4148 at R7 as shown in Figure 4.

Refer to Figure 6.

- ☐ Place the floppy controller board component side up, connector facing you.
- ☐ Place a 1N4148 diode around the 4.7K resistor previously removed.
- ☐ Insert and solder the 4.7K and 1N4148 at R16 as shown in Figure 6.
- ☐ Verify that the Reset/NMI modification (previously detailed) has been done.

Conclusion

Some of the details in this document may make you somewhat afraid of dynamic memories. Well, that's why 4K statics were invented. However, you must pay a premium for these more convenient static memories. First, the availability of the 4K statics is very limited. Second, the statics are much more expensive, often by a factor of 2 or 4 to 1. Third, the dynamics take much less power, sometimes as small as 1/10 the current. This results in smaller power supplies, less heat for smaller fan requirements and greater dependability. The savings in case size over 1K statics is very impressive, 2 cards vs. 8 cards. The 32K dynamic card has had more testing than any of the other Digital Group memory cards to assure perfect operation.

Digital Group 32K Dynamic Memory Parts List

Label	Description	Qty.*	Part #
IC00-77	4027-3 4Kx1 dynamic RAM	64(32)	072-008
IC78	8T97B, tri-state buffer	1	075-052
IC81	7404, hex inverter	1	075-004
IC83	74L04, hex inverter	1	075-049
IC87,IC92	74S08, quad 2-input AND gates	2	075-068
IC84	7410, triple 3-input NAND gates	1	075-009
IC91	7442, 1 of 10 line decoder	1	075-016
IC85,IC86,88,89	74125, tri-state buffers	4	075-031
IC90	7475, quad latches	1	075-020
IC79, IC80	74L157, quad data selector/multiplexer	2	075-067
IC82	74193, synchronous up/down counters	1	075-041
C1	100 pfd, mica capacitor	1	018-003
C2	330 pfd, mica capacitor	1	014-019
C83-95	.01 mfd, ceramic disc capacitor	13(9)	014-002
C3-42,43-82	.1 mfd, ceramic disc capacitor	80(40)	014-008
IC81,83,84,85,86, 87,88,89,92	14-pin DIP sockets	9	060-001
RPI-3,IC78,79,80,82, IC00-77,IC90,91	16-pin DIP sockets	73(41)	060-002
SIP1	10-pin SIP,2.2K resistor pack	1	008-006
RP1,RP2,RP3	16-pin DIP 33 ohm resistor pack	3	008-007
R2,R4,R5,R6	33 ohm, ¼ watt resistor	4	001-069
R1,R3	2.2K ohm, ¼ watt resistor	2	001-029
	Printed Circuit Board	1	090-060
	32K dynamic memory card documentation	1	298-119
System Modification Parts			
	7400, quad 2-input NAND gates	1	075-000
	1N4148 silicon diode	2	040-006
	3 feet of #30 insulated wire	3	110-010

*** ( ) indicates 16K version quantity.**

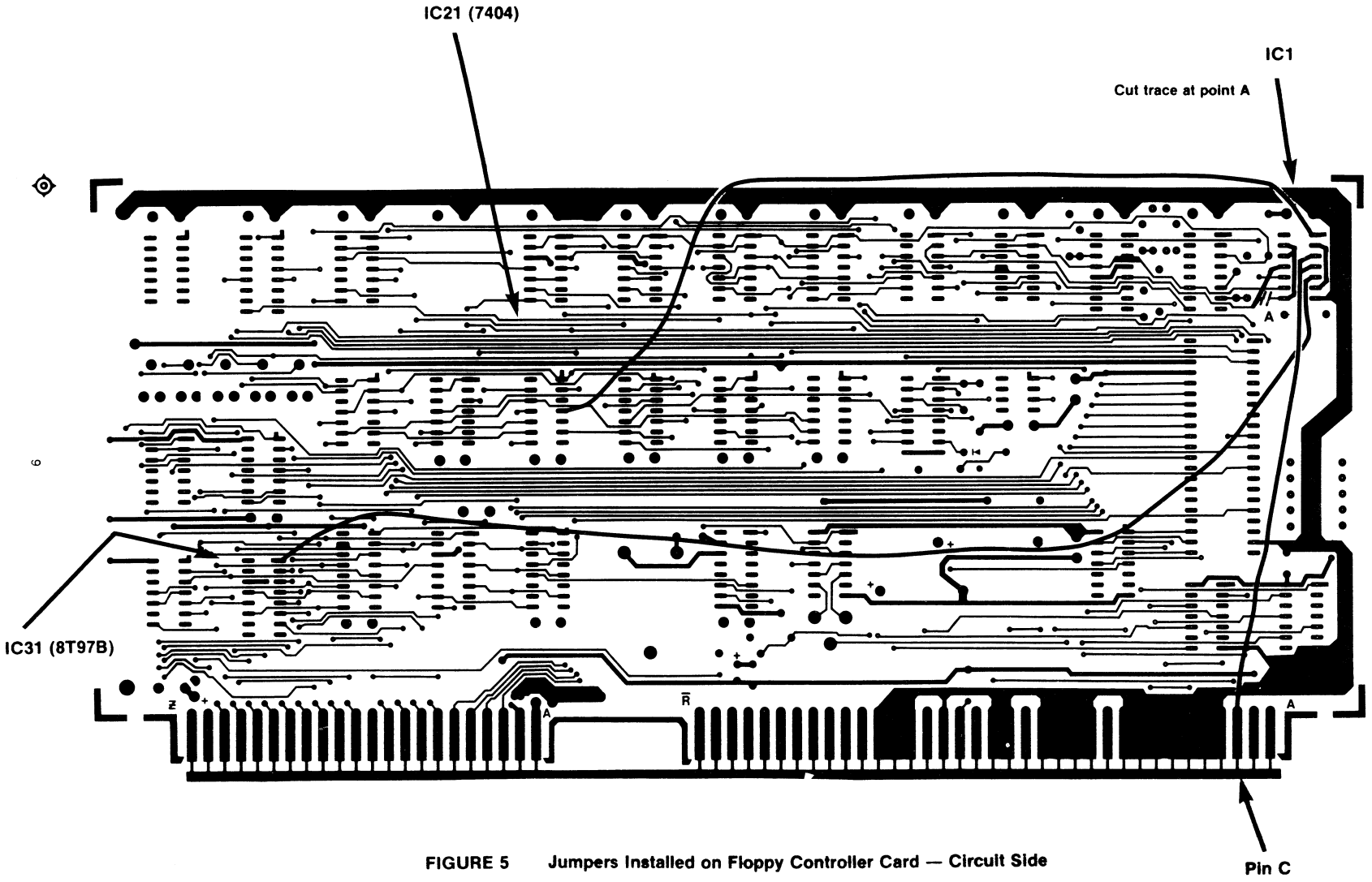
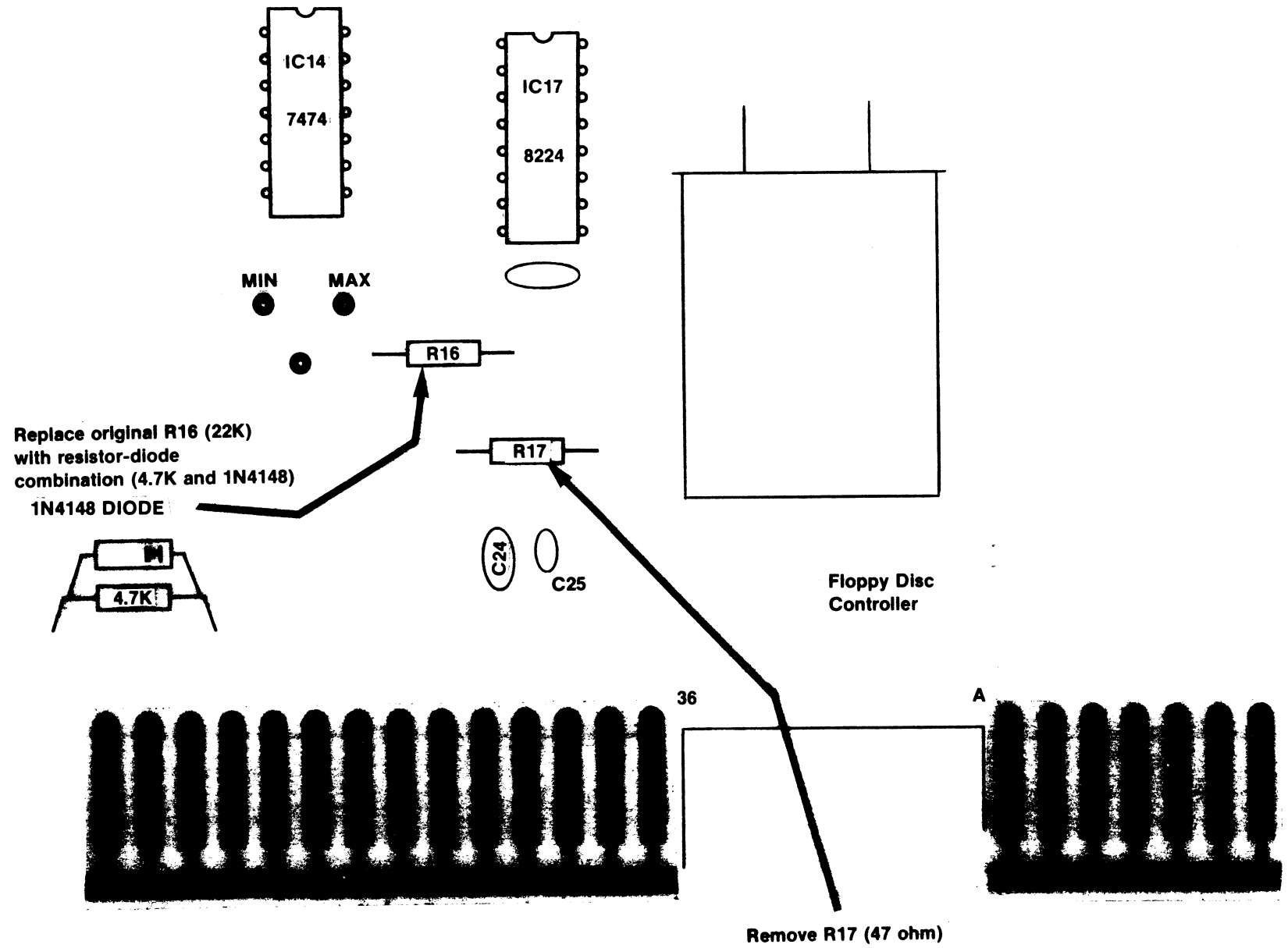


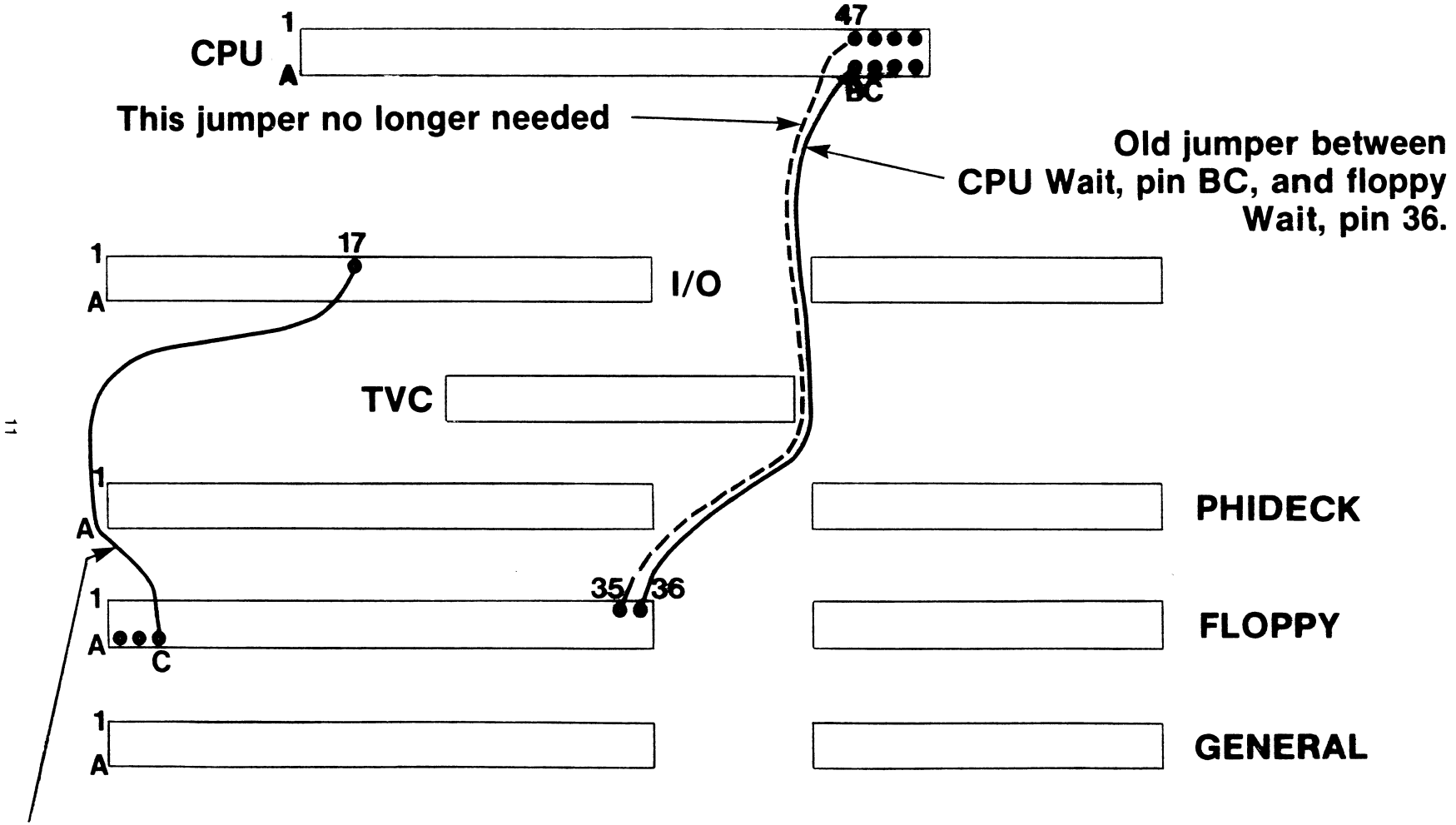
FIGURE 5 Jumpers Installed on Floppy Controller Card — Circuit Side

IC Change: IC1, 7408 to a 7400 IC



GURE 6 — FLOPPY CONTROLLER CARD MODIFICATION (Component Side)

FIGURE 7 — MOTHERBOARD MODIFICATION TO RUN DYNAMIC MEMORY



the digital group
po box 6528 denver, colorado 80206 (303) 777-7133

Dynamic Memory Test

The dynamic memory test is a modification of the "New Memory Test #2" and was primarily designed to avoid some internal Z-80 problems that only occurred when using dynamic memories. In addition, a new system was devised that permits much faster cycling of the memory test, particularly when using smaller amounts of memory. This memory test resides in the lowest 3K of memory.

Operation

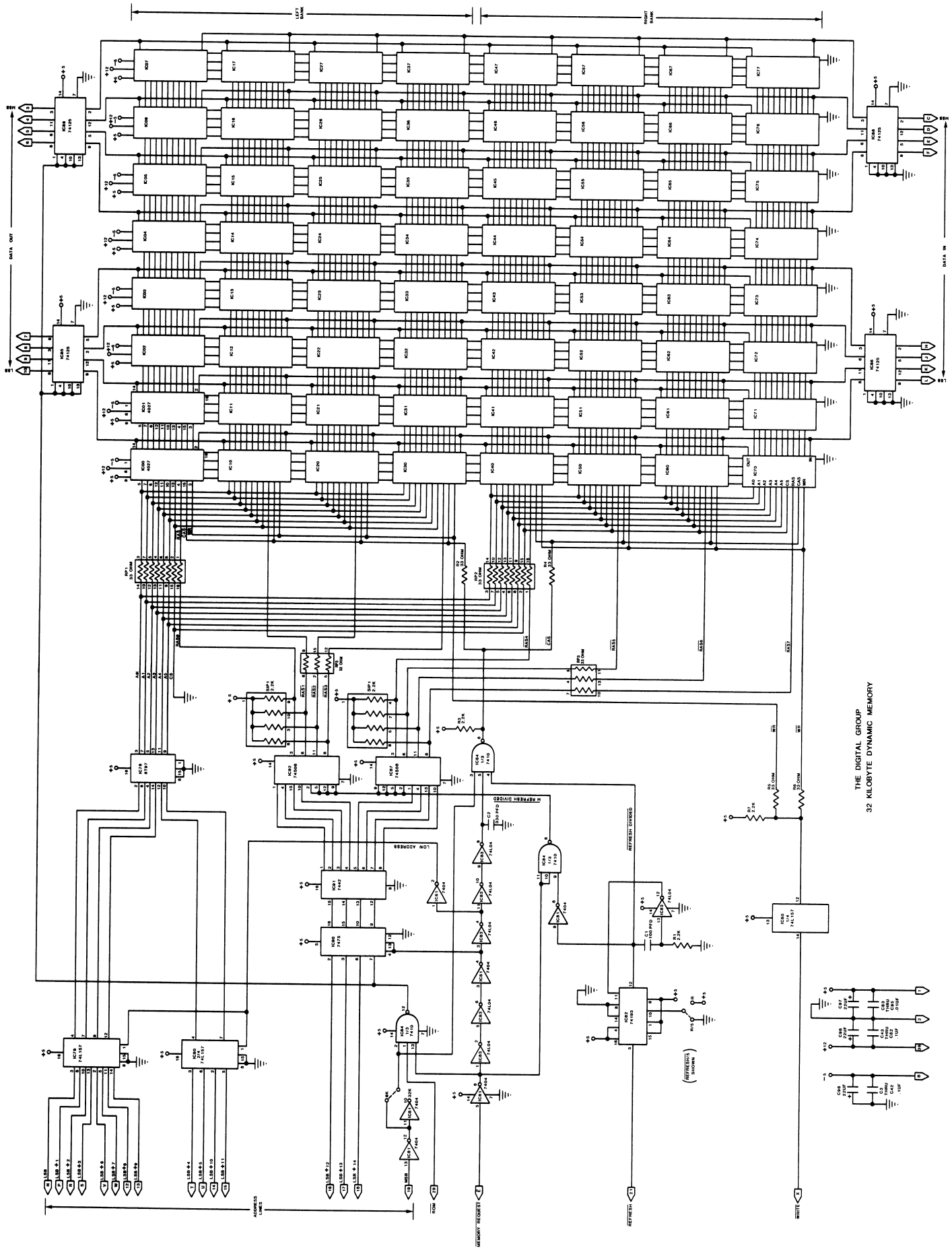
The dynamic memory test is supplied on audio cassette, but may be loaded onto Phideck or disk (and should be) for occasional testing. Read in the cassette. When the tone stops, select option "7".

You will note that two versions of the memory test are included. The first version allows the user to set the starting and stopping page address (in octal) which will be tested. The running address will not be displayed, only the successful completion of a pass or the error statistics. Since the memory test occupies 3K, the lowest possible starting page is 012 (octal). The highest possible ending page is 000 (octal). The test will reject an invalid address and request another entry.

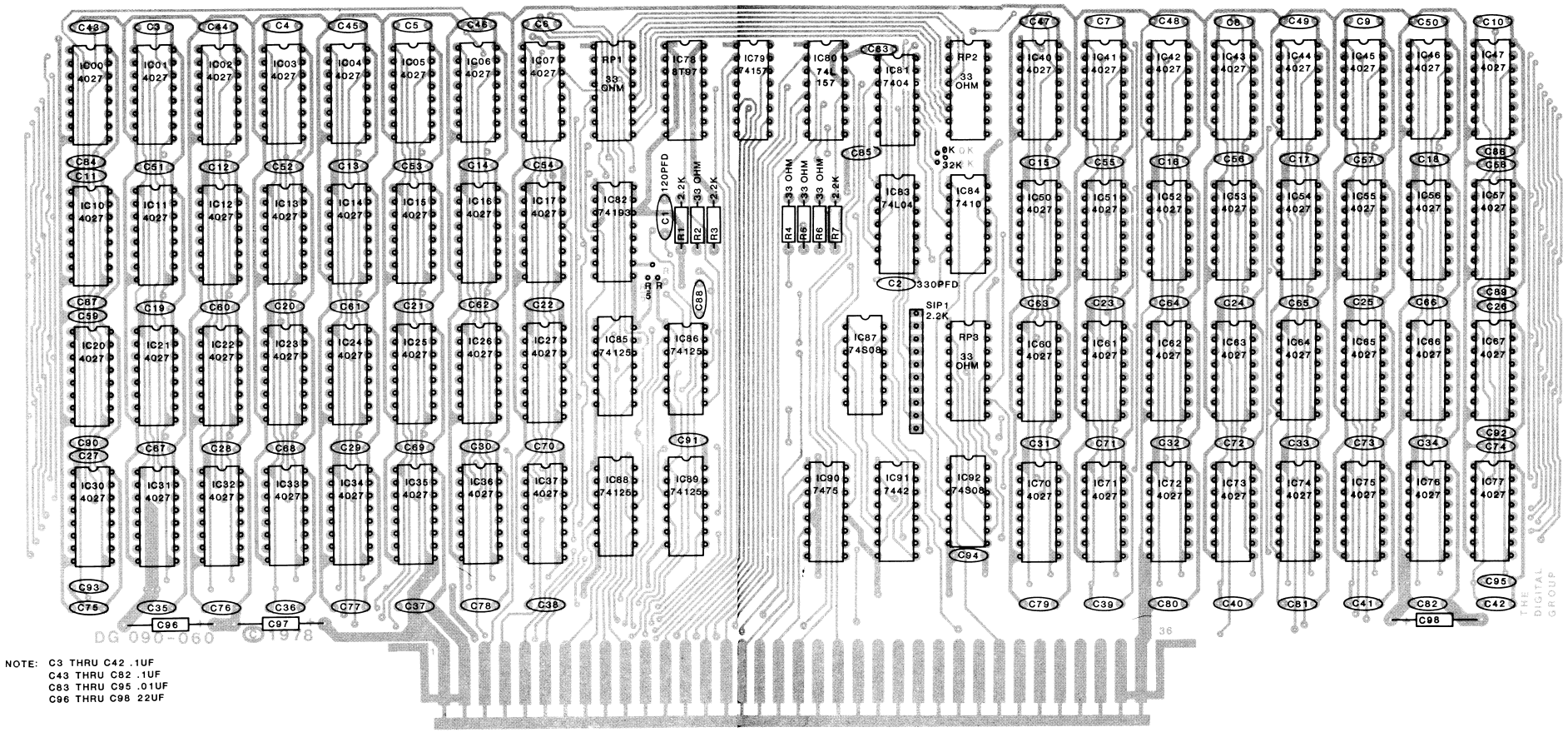
The second version will automatically set the limits to page 012 (octal) starting and 000 (octal) ending. The address being tested will be displayed.

I would suggest running this memory test whenever any strange software problem arises, as well as before beginning a large software development session. This test will run equally well on static or dynamic memories.

Dr. Robert Suding


THE DIGITAL GROUP
32 KILOBYTE DYNAMIC MEMORY
LEFT BANK
RIGHT BANK
DATA OUT
DATA IN
ADDRESS LINES
MEMORY REQUEST
REFRESH
WRITE
ROW
REFRESH DIVIDED
LOW ADDRESS
M REFRESH DIVISOR

32 KILOBYTE DYNAMIC MEMORY



NOTE: C3 THRU C42 .1UF
C43 THRU C82 .1UF
C83 THRU C95 .01UF
C96 THRU C98 22UF